Safe-Operating Areas (SOAs) for Reliable High-Voltage Analog Devices

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Many Uses For High-Voltage Analog

Escalating Need

- ☐ Battery Charging
- ☐ Potable Products
- ☐ Microprocessors
- ☐ Converters
- ☐ Controllers
- ☐ Etc

1 – 20 V

- ☐ Automotive
- ☐ Printers
- ☐ Audio
- ☐ Converters
- ☐ Controllers
- ☐ Etc

20 – 80 V

- ☐ Consumer
- ☐ Power Supplies
- ☐ Automotive
- ☐ Converters
- ☐ Controllers
- ☐ Etc

80 – 120 V

- ☐ Industrial
- ☐ Medical
- ☐ Displays
- ☐ Converters
- ☐ Controllers
- ☐ Etc

> 120 V

How to Safely Integrate with Low-Voltage CMOS ?

Fundamental Reliability Physics Limitations

Fundamental Device Operational Issues at t=0

- Silicon Avalanche Breakdown Field : 0.2-0.8 MV/cm
- SiO_2 Breakdown Field: 10-15 MV/cm
- Melting Temperature of Metals: Al(660°C) , Cu(1083°C)
- Fusing Current Density for Metals: ~ $2x10^7A/cm^2$
- BVdss and BVii Limitations
- Latch-Up /ESD

Fundamental Device Reliability Issues for TF=10yrs@105°C

- Electromigration (EM)
- Stress Migration (SM)
- Time-Dependent Dielectric Breakdown (TDDB)
- Hot Carrier Injection(HCI)
- Negative-Bias Temperature Instability (NBTI)
- Power Density and Power Dissipation Issues
- Single-Event Upsets

Safe-Operating Areas (SOAs)

☐ Electrical SOA (e-SOA)

- Short Term Issues: BVdss, BVii, Latch-up, ESD

☐ Thermal SOA (T-SOA)

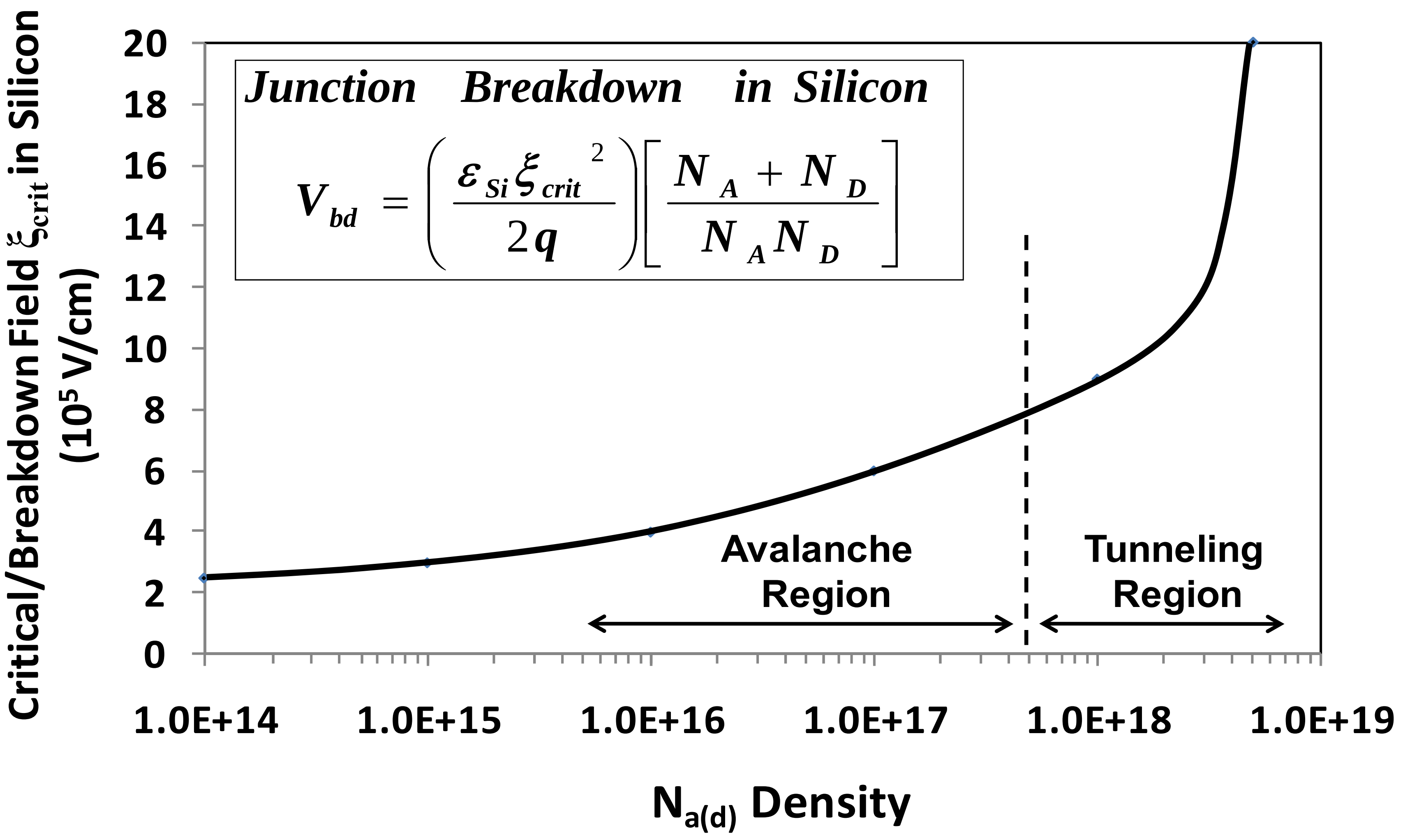
- Medium Term Issues: Power Density and Dissipation

☐ Reliability SOA (R-SOA)

- Long Term Issues: TDDB, HCI, NBTI, EM, SM, SEU

e-SOA

Critical Electric Field for Avalanching in Silicon



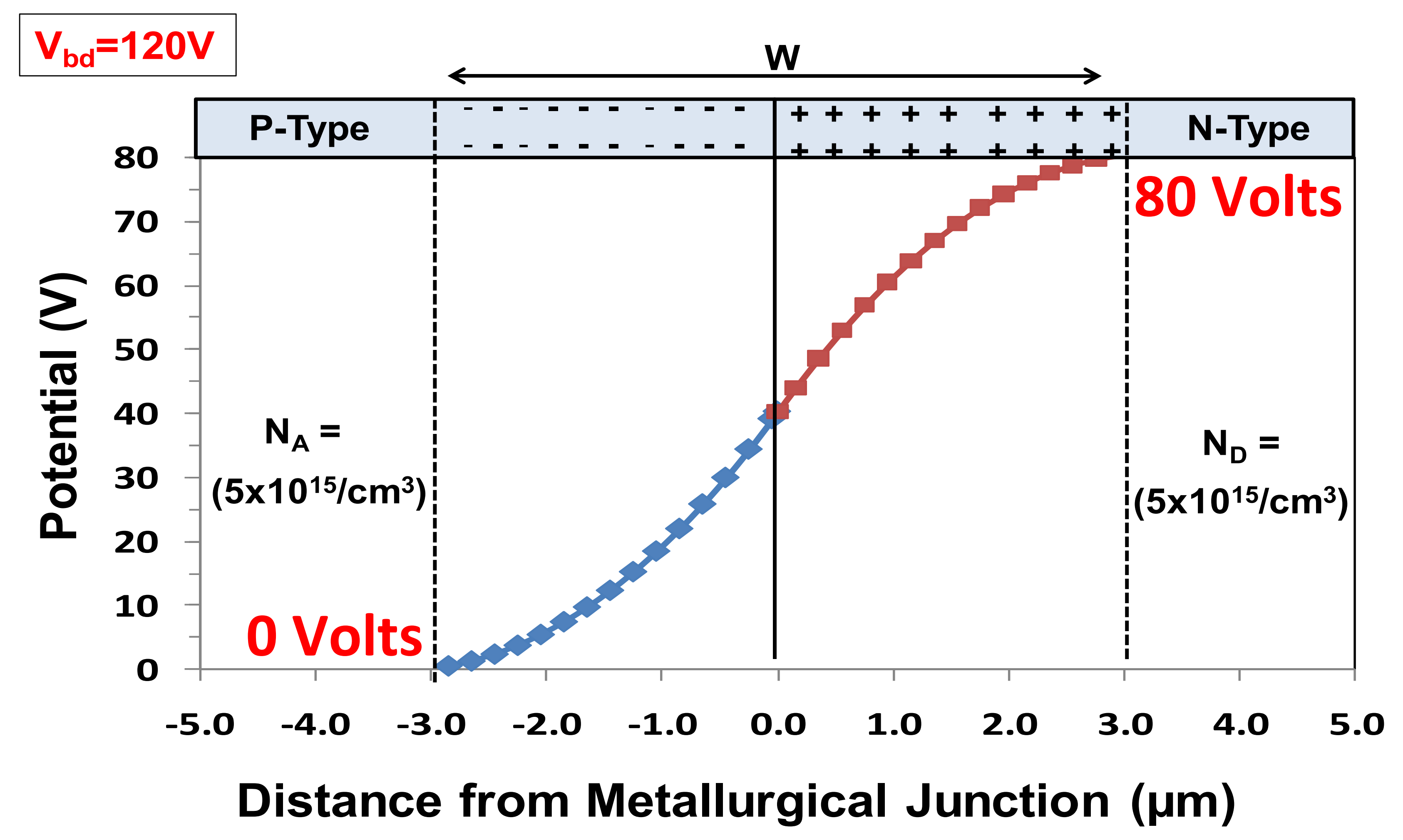
Junction Breakdown in Silicon

$$V_{bd} = \left(\frac{\varepsilon_{Si}\xi_{crit}^{2}}{2q}\right)\left[\frac{N_A + N_D}{N_A N_D}\right]$$

Critical field (~0.2-0.8MV/cm) for avalanching must be avoided !

e-SOA

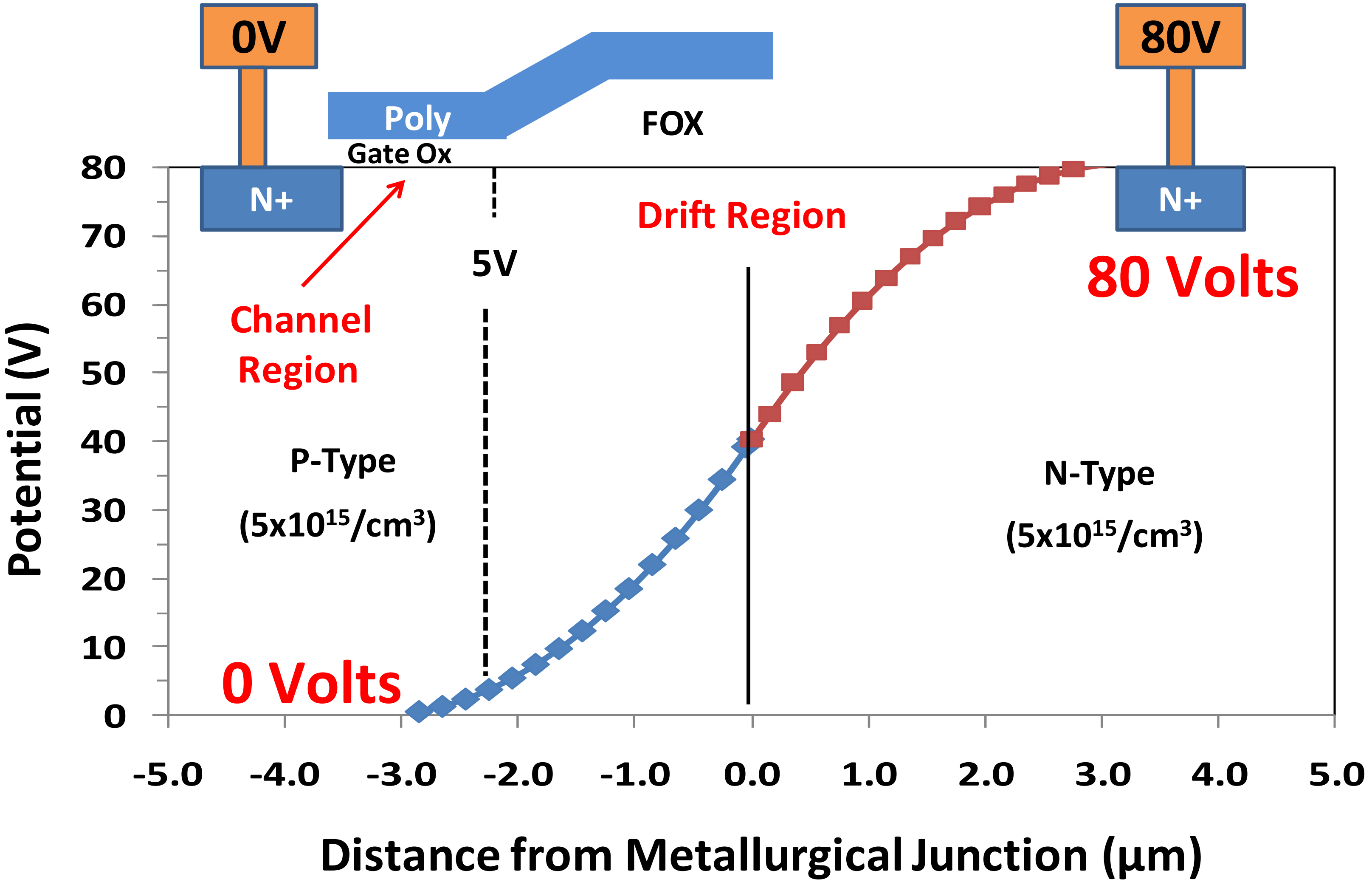
Voltage Drop Across Junction Depletion-Region



Can safely drop large voltages across junction depletion-regions

e-SOA

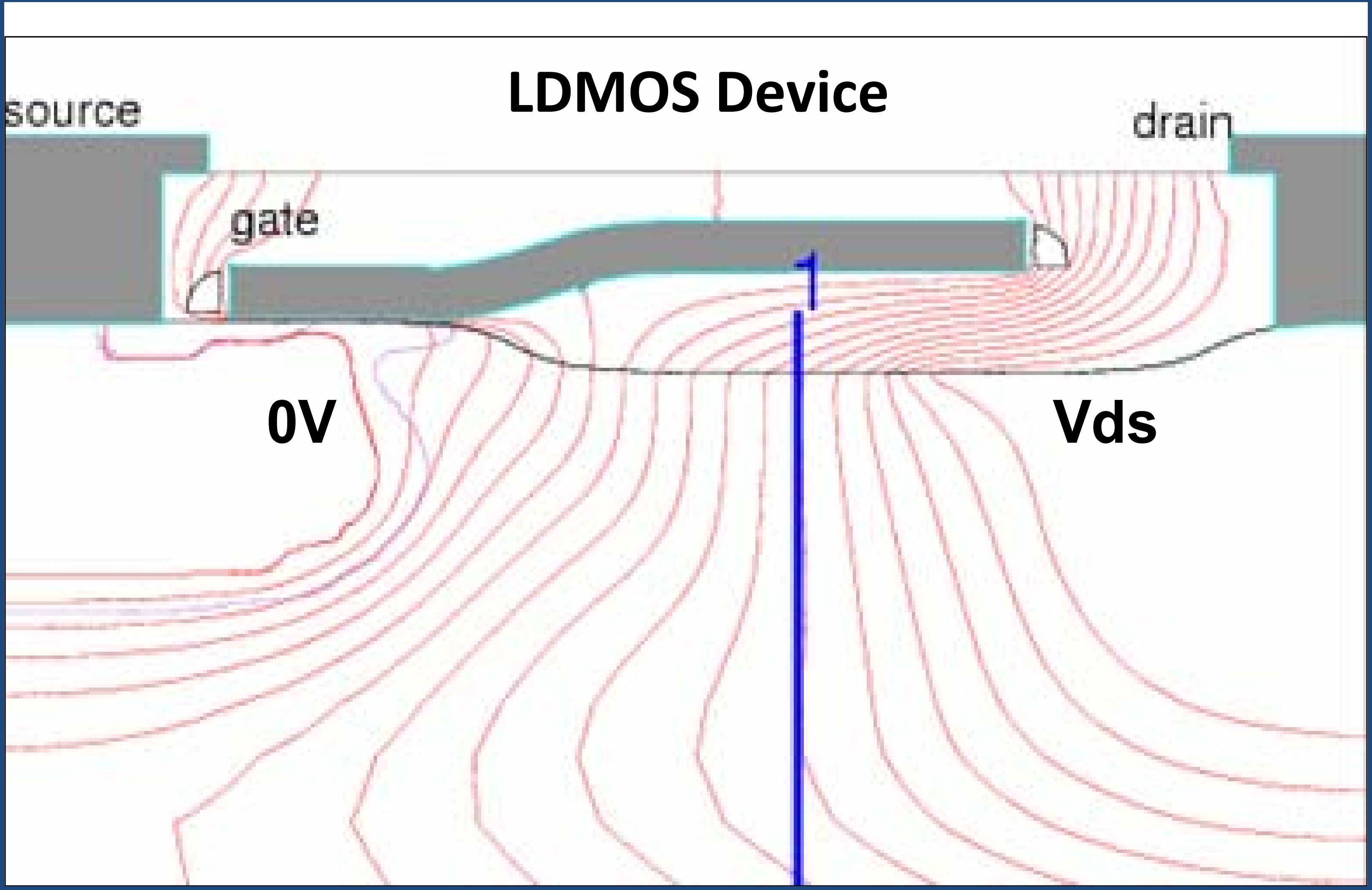
5V-CMOS with 80V Drain Extension



Note: Most voltage dropped before reaching gate

e-SOA

Full Simulation of Voltage Drop

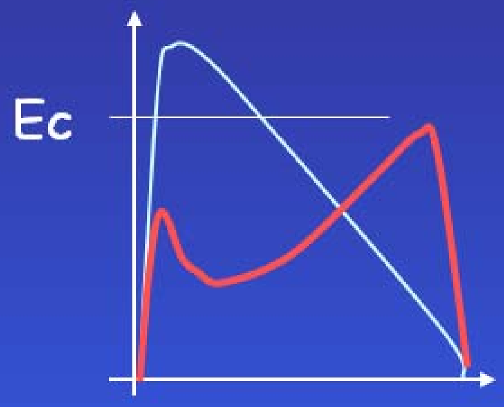


Note: Voltage drop from drain to source

e-SOA

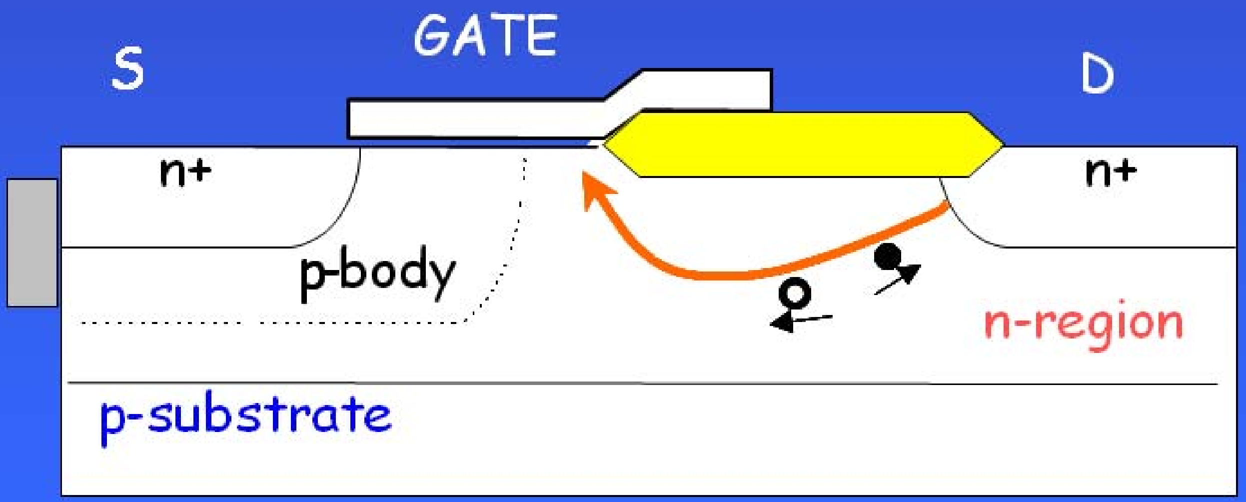
(Snapback/Breakdown) Performance

BVii

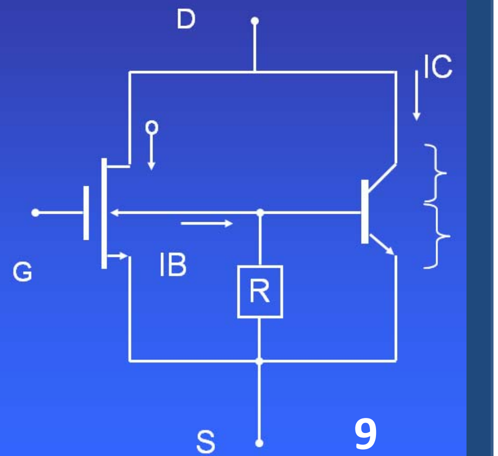


as current increases, field peaks at drain, leading to snapback

Vds = constant



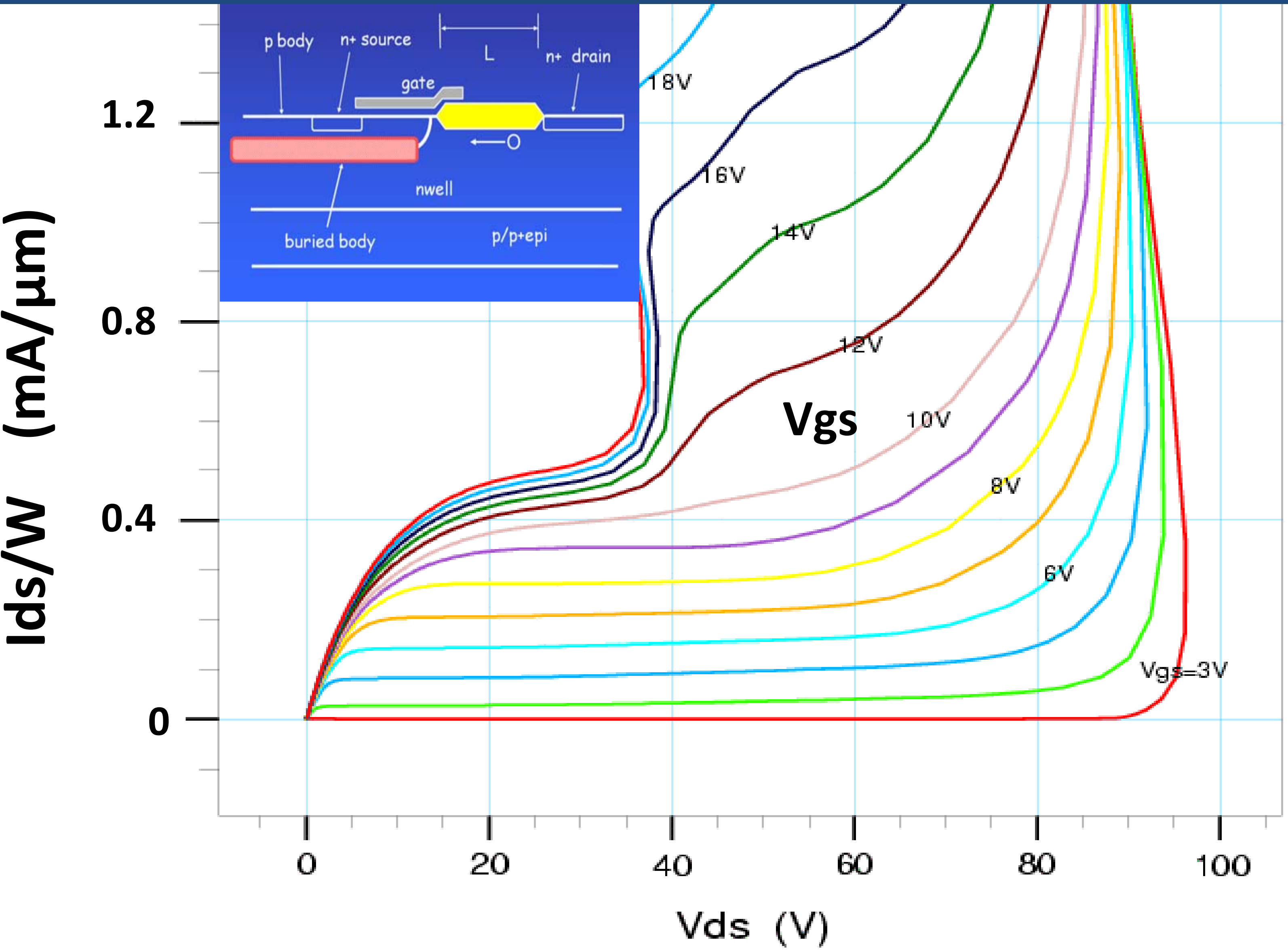
Parasitic Bipolar



Note: Parasitic Bipolar Turn On

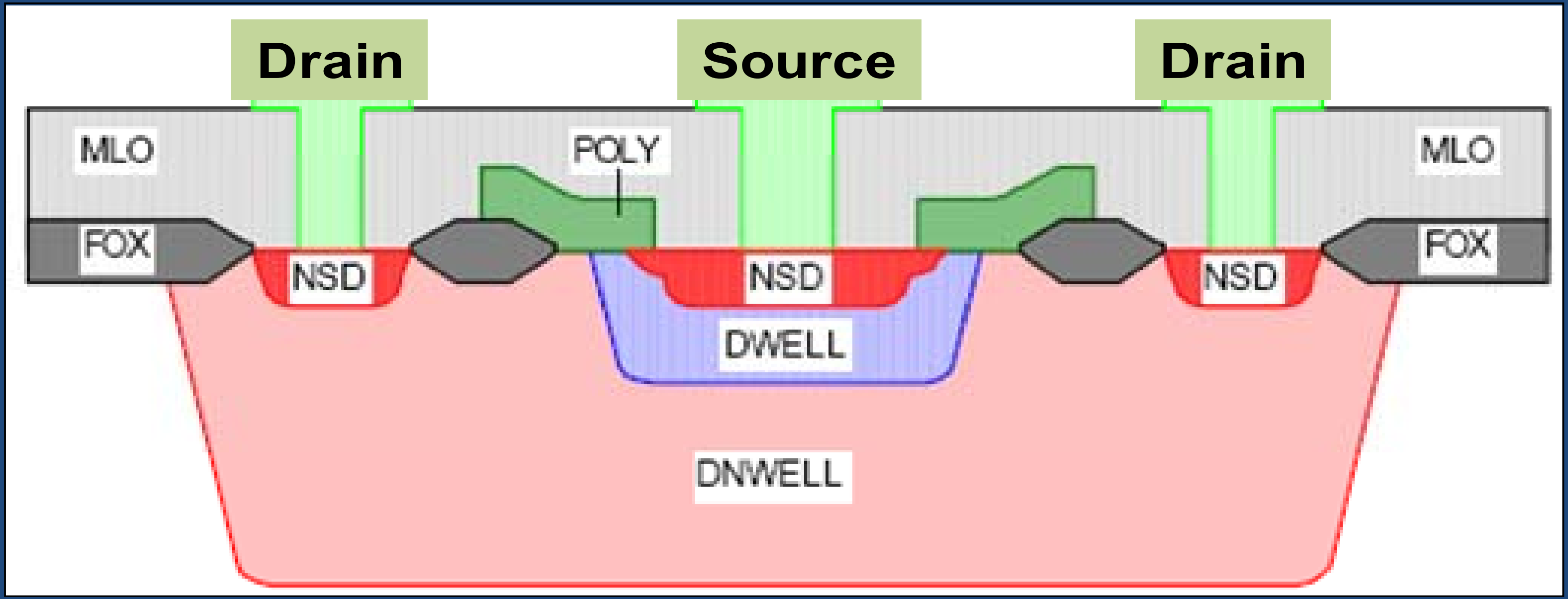
e-SOA

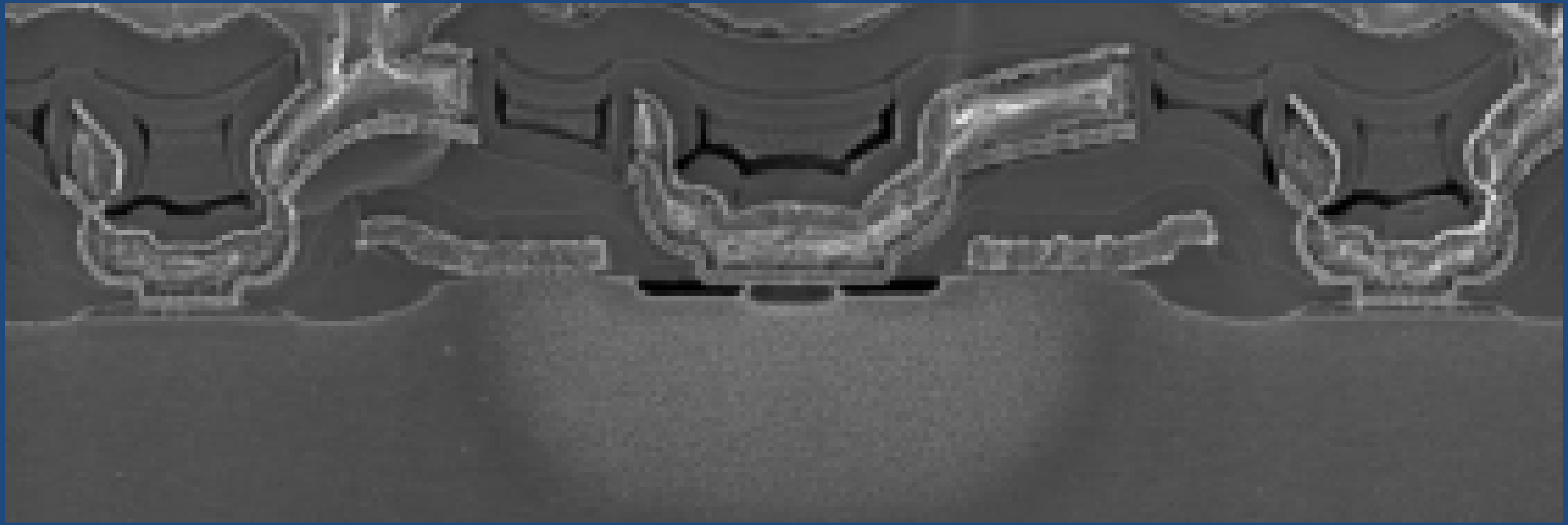
Improving BVii Performance



e-SOA

Fully Integrated LDMOS Device





What About Long-Term Reliability?

Now that we know how to build H-V devices in low-voltage CMOS that work safely at time zero (e-SOA) --- will they last for 10 yrs at 105ºC?

Other Considerations:

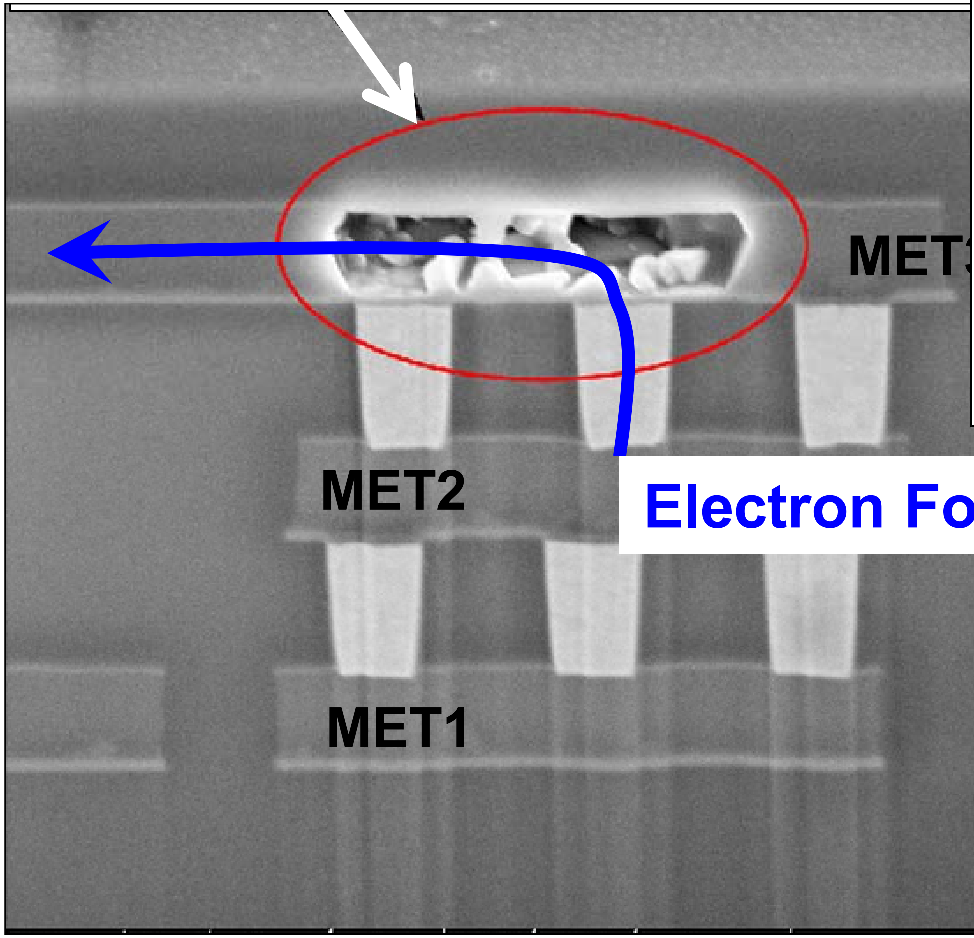
- ☐ Thermal SOA (T-SOA)
- ☐ Reliability SOA (R-SOA)

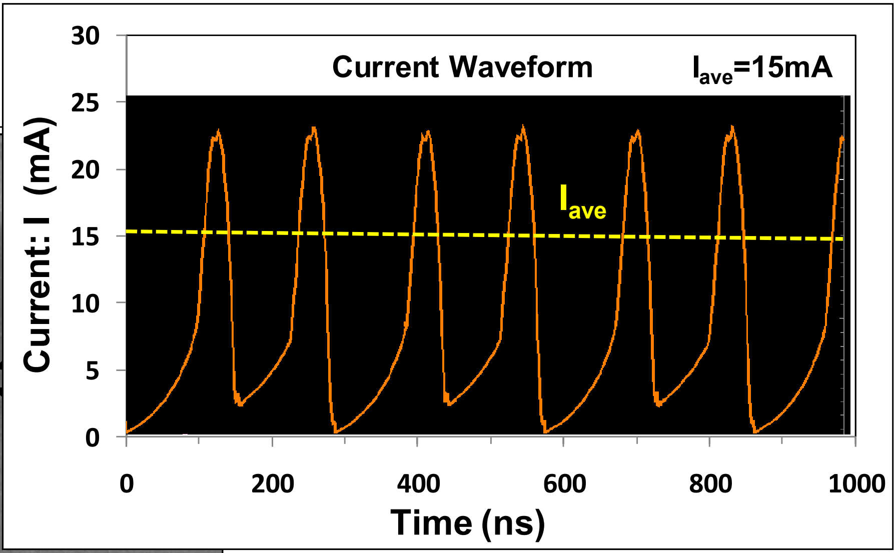
T-SOA

Electromigation in a Power Interconnects

3um wide conductor with 9 vias

Electromigration-Induced Voiding





$$J_{Ave} = \frac{15mA}{(3.0\mu m)(0.5\mu m)}$$

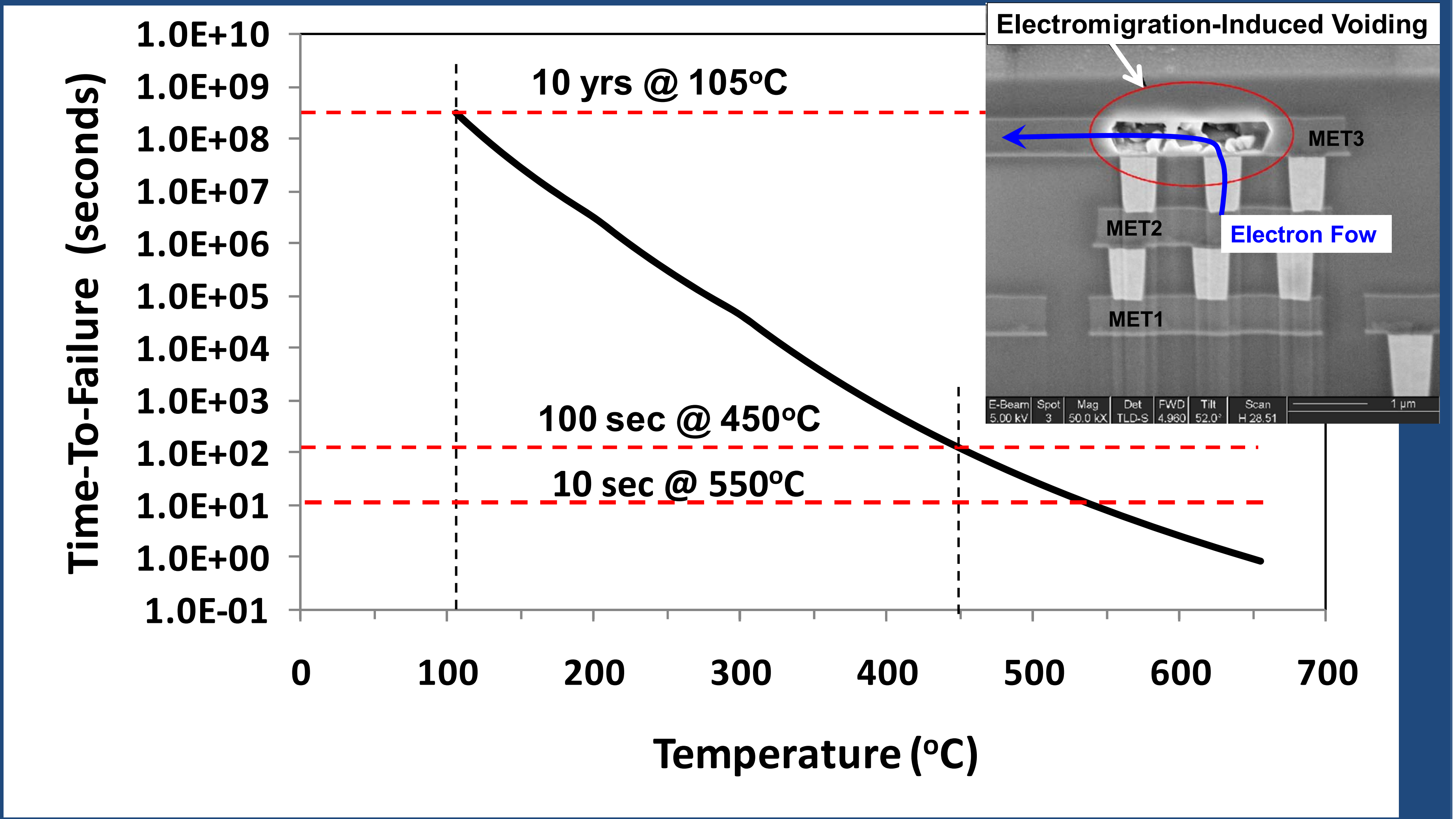
$$= 1MA/cm^2$$

$$Temp = 179^{o}C$$

$$TF = 400\ hrs$$

T-SOA

Metal Electromigration Lifetime Versus Temperature

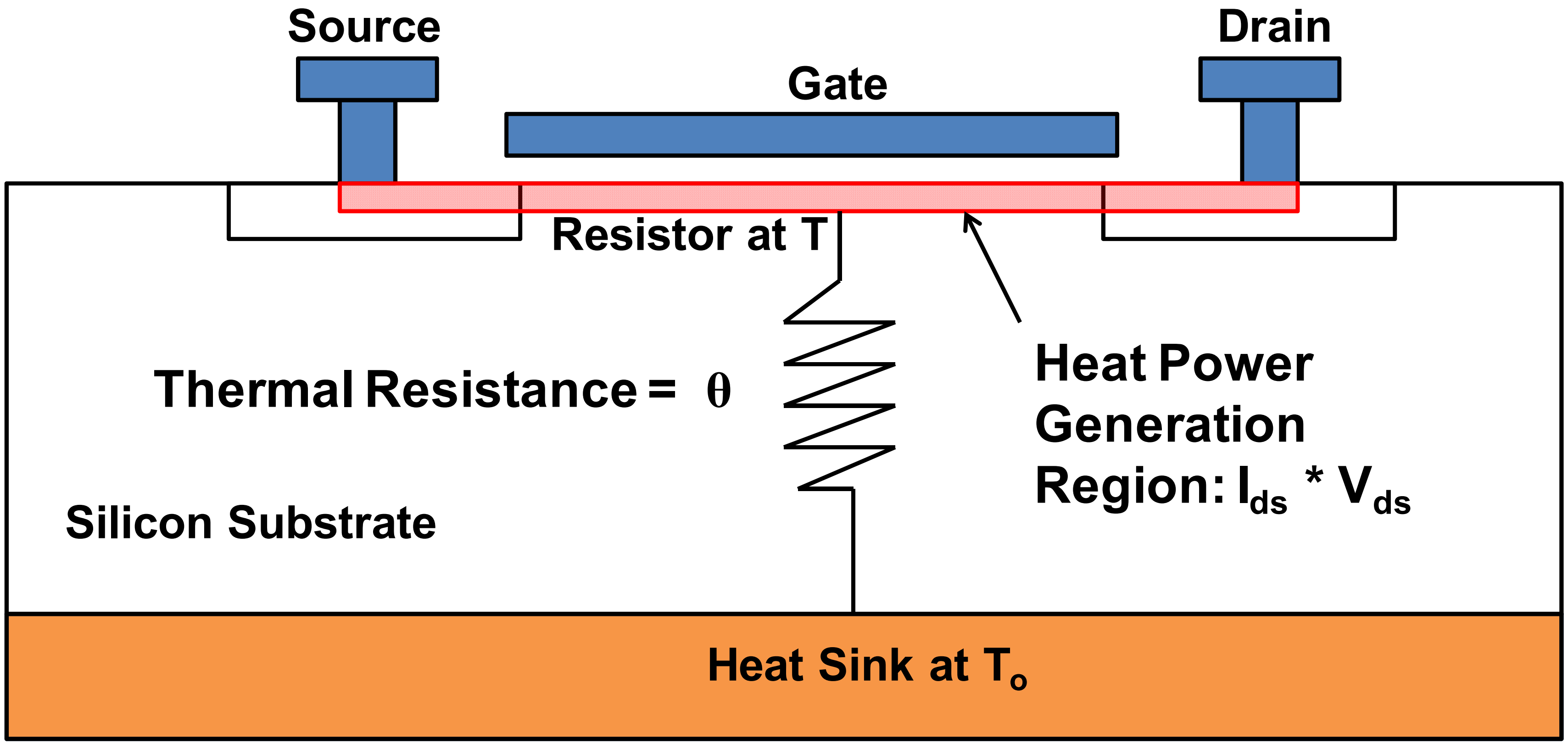


Note: Metal migration (normally requiring 10yrs at 105°C) occurs within ~100sec at 450°C or ~10sec at 550°C.

T-SOA

Steady State Heat Flow

Remember ---- for Joule heating analysis, the MOSFET is simply a Gate-Controlled Resistor



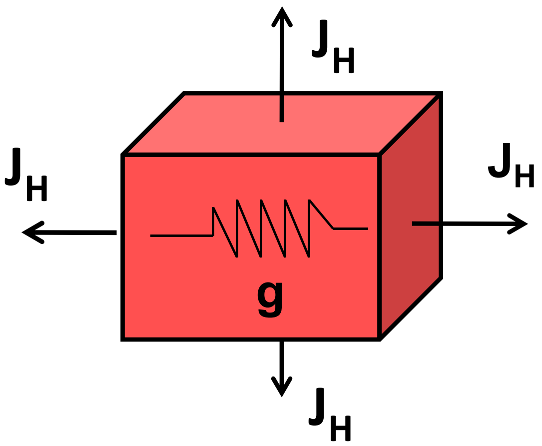
In Steady State: $\Delta T = \theta \bullet Power = \theta \bullet (I_{ds} V_{ds})$

Thermal resistance θ is normally expressed in °C/Watt

T-SOA

Transient Heat Flow

Heat Generation = Heat Absorbed + Heat Transferred



g = generation of heat per unit volume $= J_Q E$

J_H = flux of heat out of unit volume

Conservation of Energy:

Power Density Input = Power Density Absorbed + Power Density Transferred

$$\boxed{g(t) = \rho c \frac{\partial T}{\partial t} + \vec{\nabla} \bullet \vec{J}_H}$$

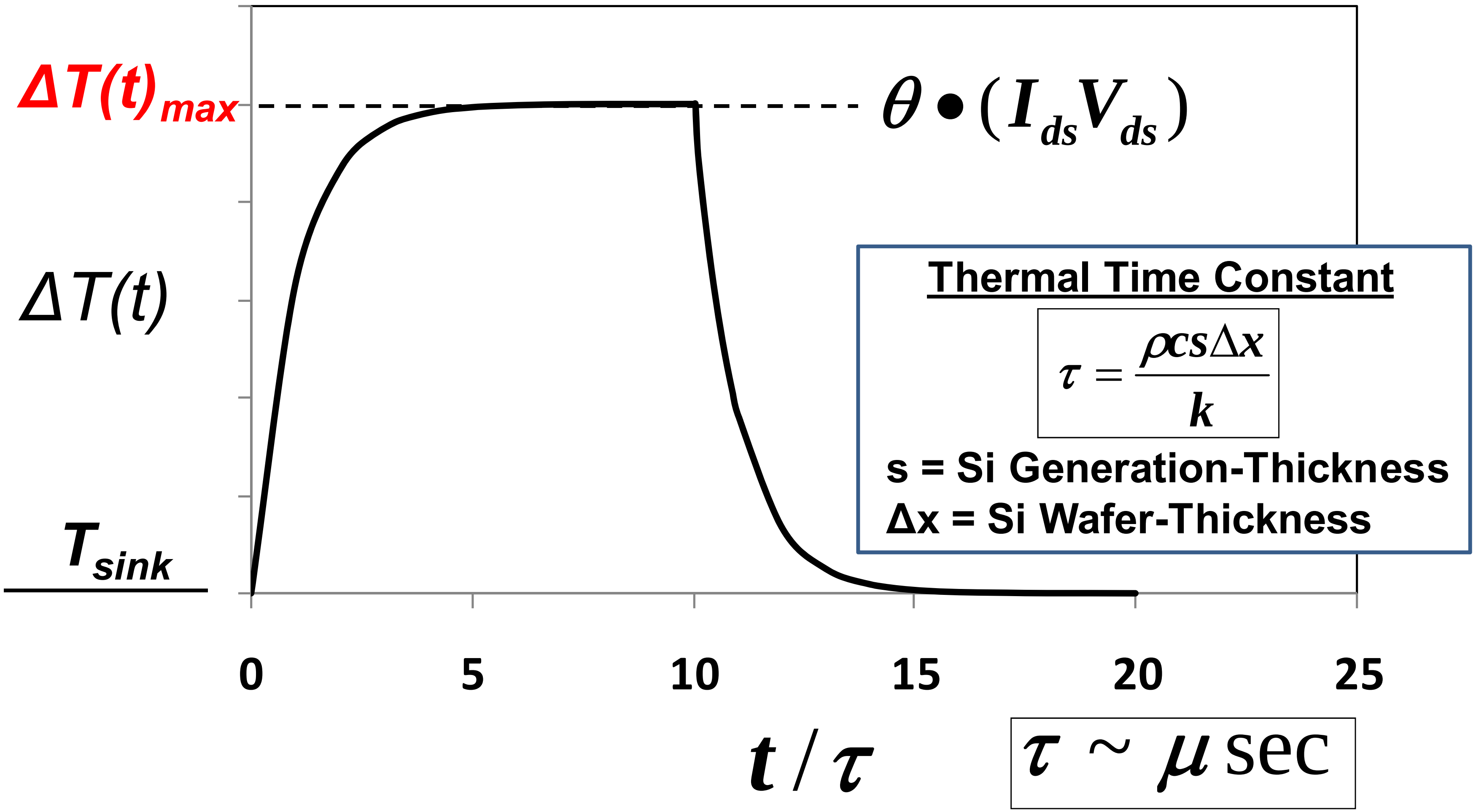
where :

$\vec{J}_H = -k\vec{\nabla}T$, k = *thermal conductivity*, c = *specific heat*, ρ = *mass density*

$$k_{Si} = 83.7 \frac{W}{{}^oC\ m}\ ;\ \rho_{Si} = 2.33x10^3 \frac{kg}{m^3}\ ;\ c_{Si} = 6.78x10^2 \frac{W\sec}{{}^0C\ kg}$$

T-SOA

Temperature Rise/Fall Times for Resistors in Silicon



Thermal Time Constant

$$\boxed{\tau = \frac{\rho c s \Delta x}{k}}$$

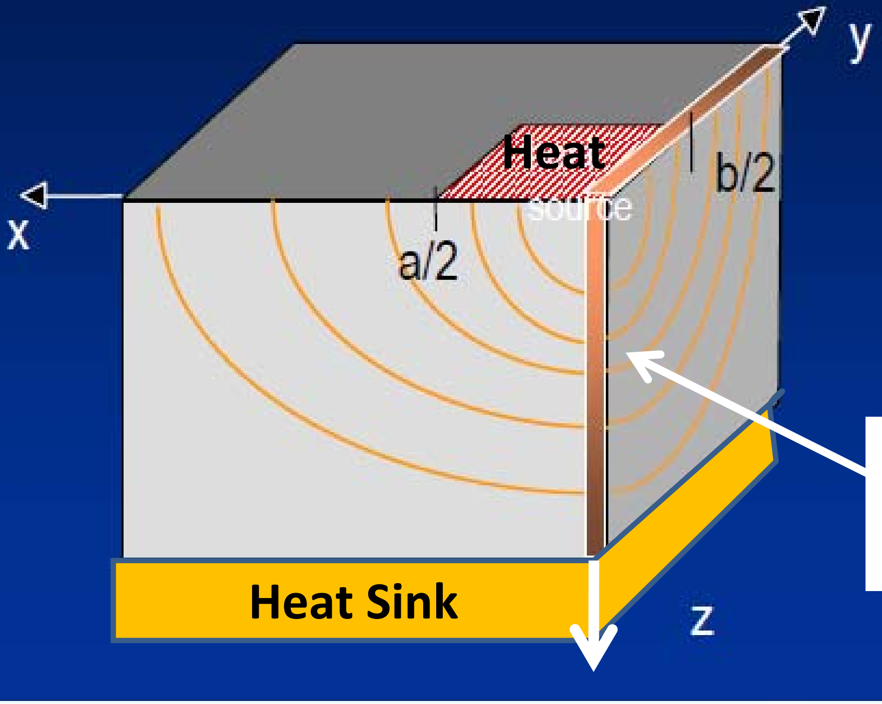
s = Si Generation-Thickness
Δx = Si Wafer-Thickness

$$\boxed{\tau \sim \mu \sec}$$

Note: 1ms pulses should reach ~ thermal equilibrium

T-SOA

Transient Thermal Modeling



k = 0.84 W/cm°C

$\alpha = k/(\rho c)$

$= 0.5\ \text{cm}^2/\text{s}$

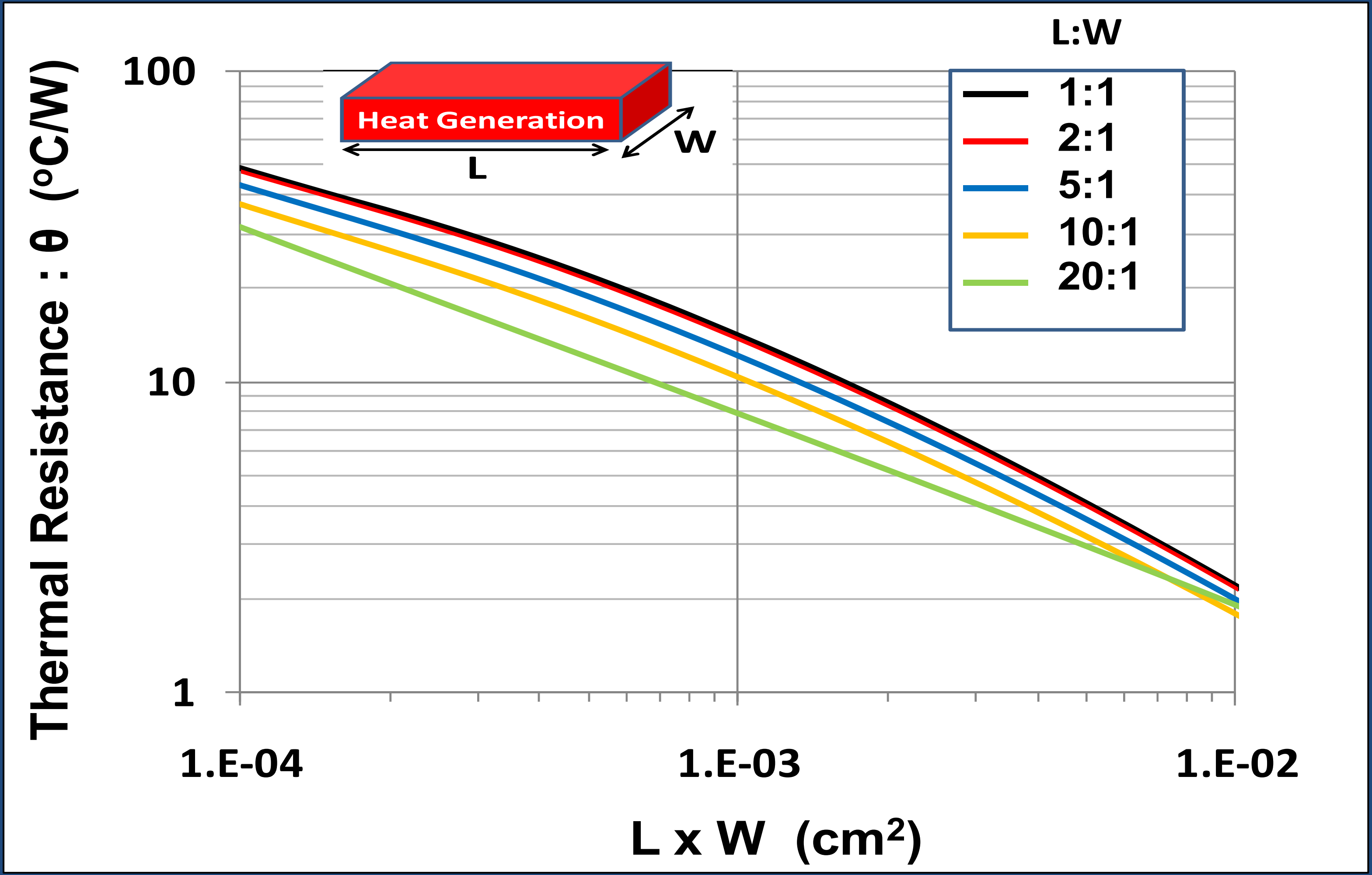
Most of Thermal-Gradient/ Heat-Flow is in Vertical Direction

$$\Delta T(x,y,z,t) = \frac{\alpha}{k}\int_0^t \frac{dP(t')}{[4\pi\alpha(t-t')]^{1.5}} \times \exp\left[-\frac{r^2}{4\alpha(t-t')}\right]dt'$$

[IEEE-TED, vol. 48, #12, Dec 2001, pp. 2796-2802]

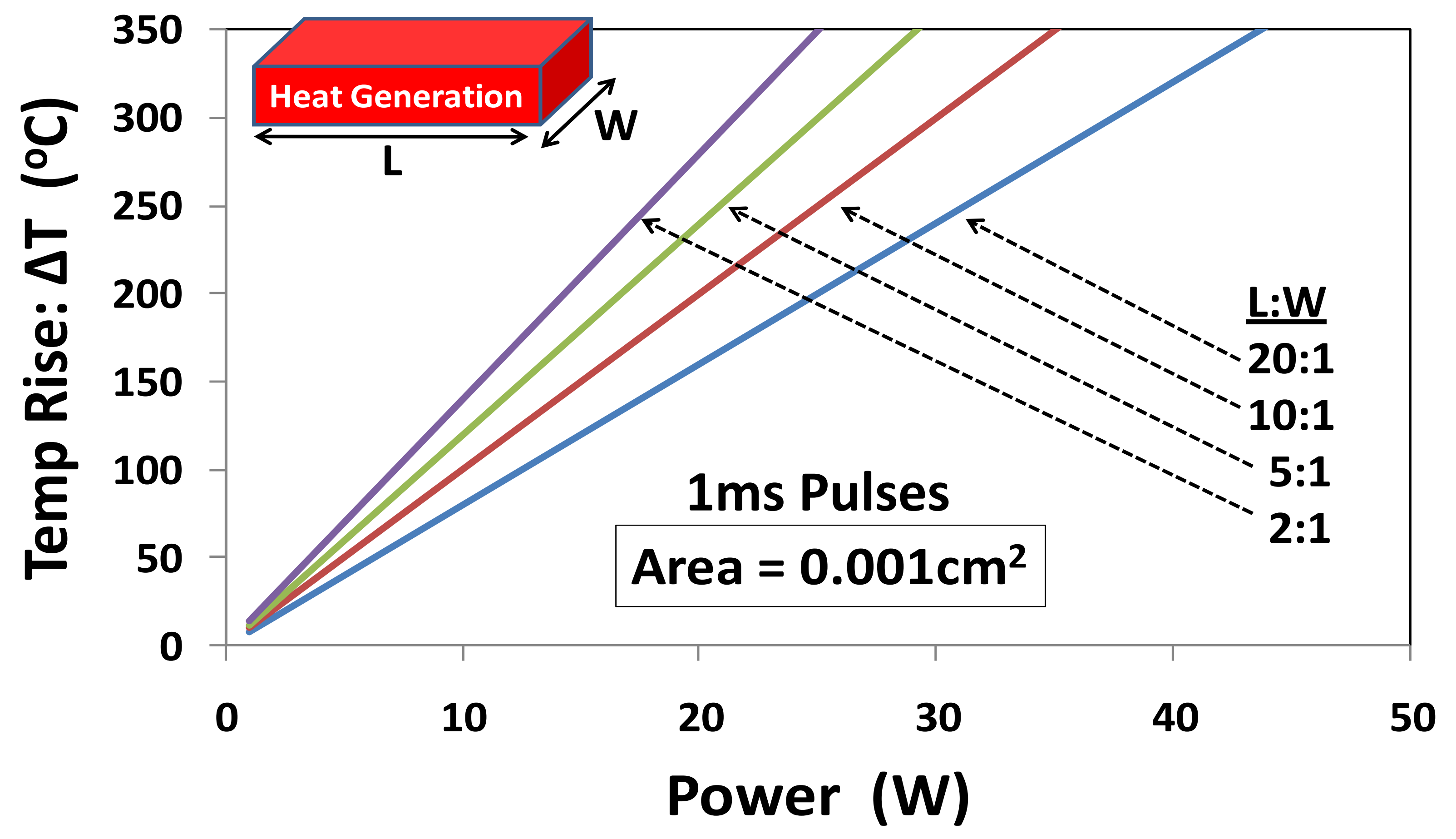
T-SOA

Modeled Thermal Resistance With 1ms Power Pulse



- ☐ Modeling of thermal resistance in agreement with experiment
- ☐ Modeling is slightly conservative, which is good!
- ☐ Thermal resistance θ defines allowed power density (T-SOA)

Thermal SOA (T-SOA)



Notes: (1) $40W/0.001cm^2 = 40kW/cm^2$

(2) LDMOS devices can have ~ MW/cm^2 capability !!

(3) $T_{metal} = T_J + \Delta T = 100^oC + 350^oC = 450^oC$

(4) Metal lifetime at 450°C is only ~100sec !

What About Long-Term Reliability?

Thus far ----

- ☐ We have learned how to generate:
  electrical safe operating areas (e-SOAs)

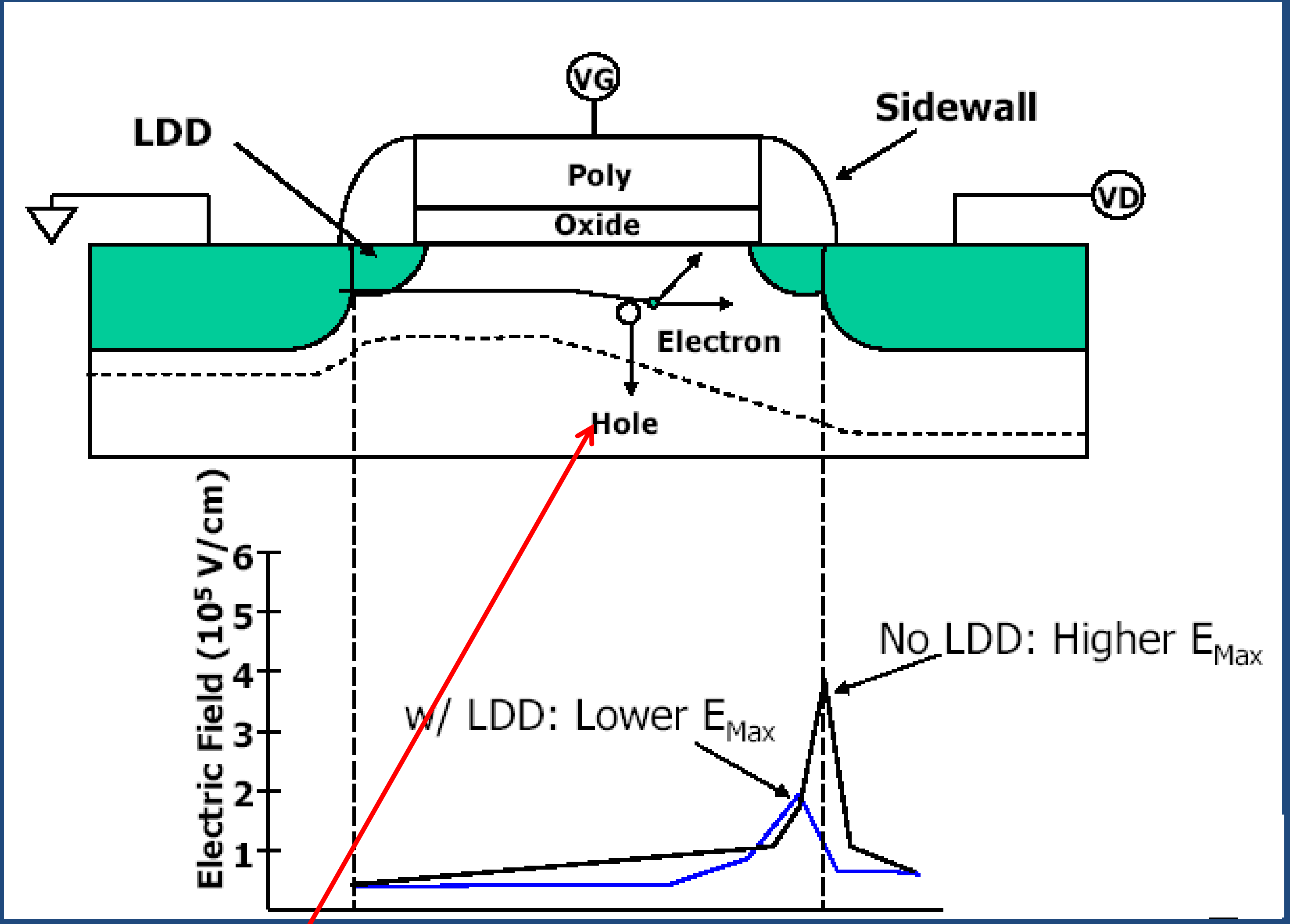
- ☐ We have learned how to generate:
  Thermal safe operating areas: T-SOAs

**Remaining --- Long Term (10yr/105°C)
Reliability Safe Operating Areas: R-SOAs**

Examples:

- ☐ Hot Carrier Injection (HCI)
- ☐ Biased Temperature Instability (BTI)
- ☐ Time-Dependent Dielectric Breakdown (TDDB)

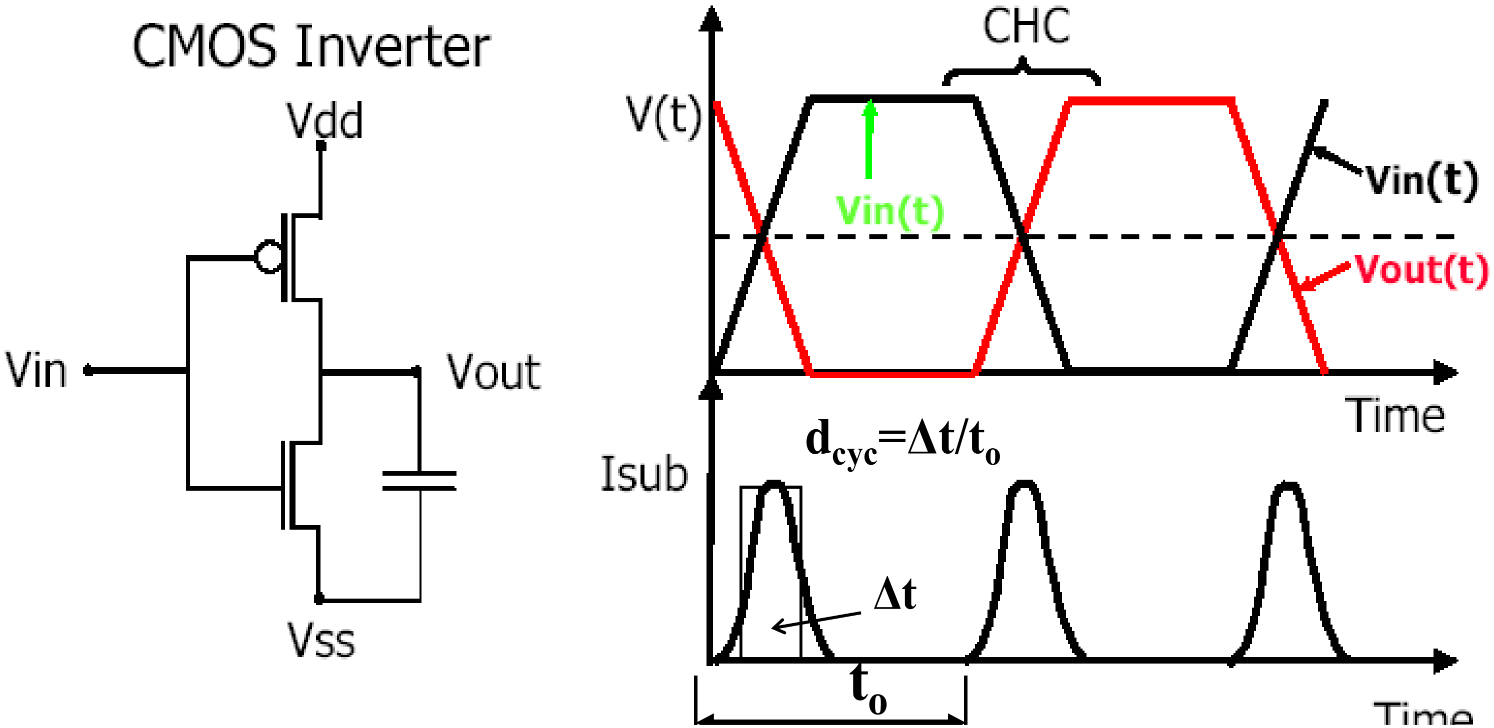
Standard CMOS Hot Carrier Injection (HCI)



Note: Substrate current is a good proxy for HCI stress

R-SOA

HCI During Digital Circuit Operation



Isub current is generated primarily during device switching

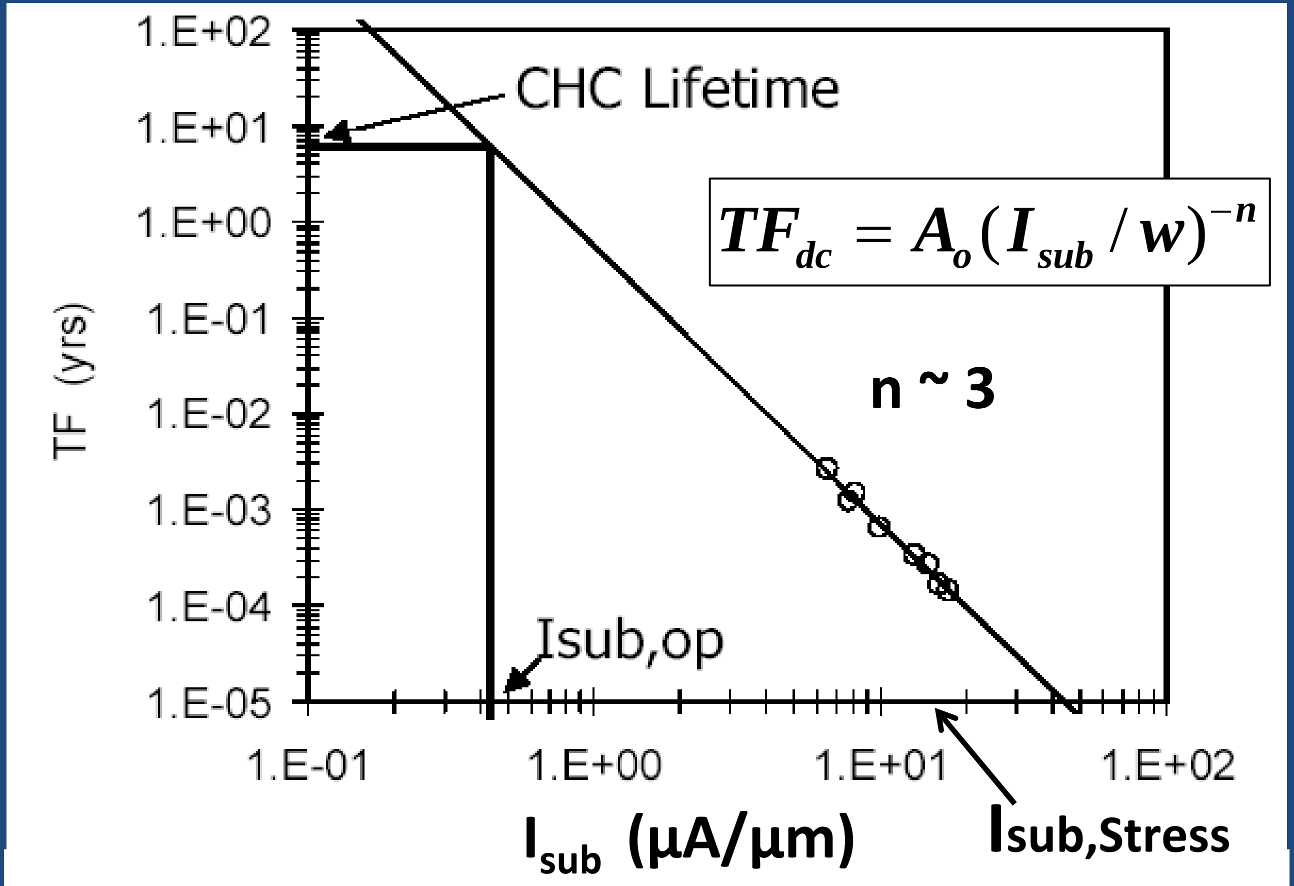
To minimize CHC:

(1) Reduce slew rate of waveform
(2) Reduce load capacitance

Note: Duty-cycle for HCI can be quite low

R-SOA

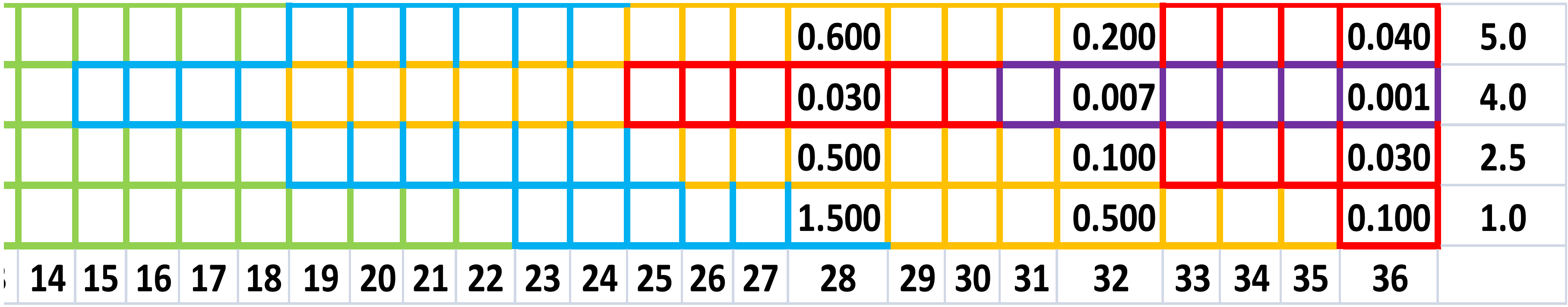
CHC Lifetime Versus Substrate Current



Problem: DEMOS/LDMOS --- difficult/impossible to measure substrate current. Must take empirical stress data.

Example:Generation of HCI-SOA for 30V LDMOS

Measured/Extrapolated DC HCI 10% Degradation Lifetime (yrs)



																							Vgs
													0.600				0.200				0.040	5.0
													0.030				0.007				0.001	4.0
													0.500				0.100				0.030	2.5
													1.500				0.500				0.100	1.0
14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	

Vds

Other Voltage Conditions can be Modeled:

$$AF_{Vds} = \exp[\beta(36V - V_{ds})]$$
$$where: \beta = 0.43/V$$

$$AF_{Vgs} = \exp[-\alpha(4V - V_{gs})^2]$$
$$where\ : \alpha = \begin{cases} 1.5/V^2 & for\quad V_{gs} \le 4 \\ 3.4/V^2 & for\quad V_{gs} \ge 4 \end{cases}$$

🟩 > 10 yrs

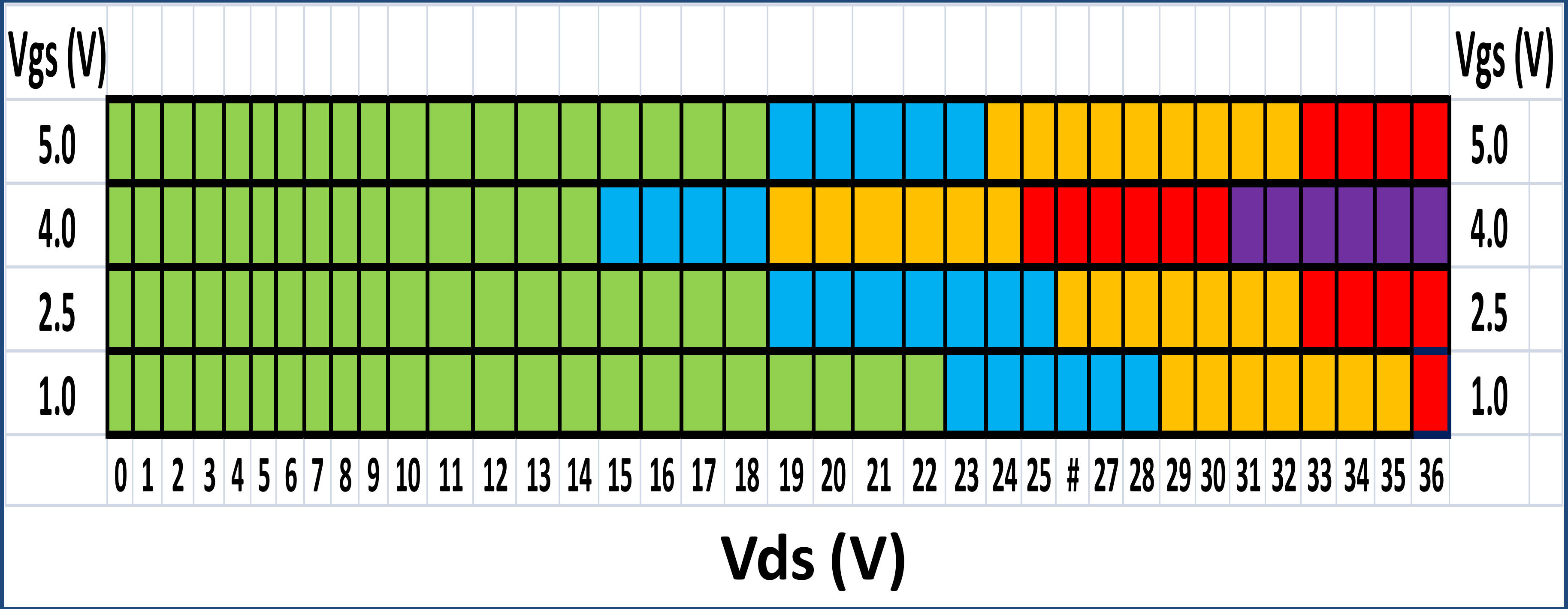
🟧 1 yr 0.1 yr

🟦 10yr 1 yr

🟥 0.1 yr 0.01 yr

🟪 0.01 yr 0.001 yr

Example:Generation of HCI-SOA for 30V LDMOS



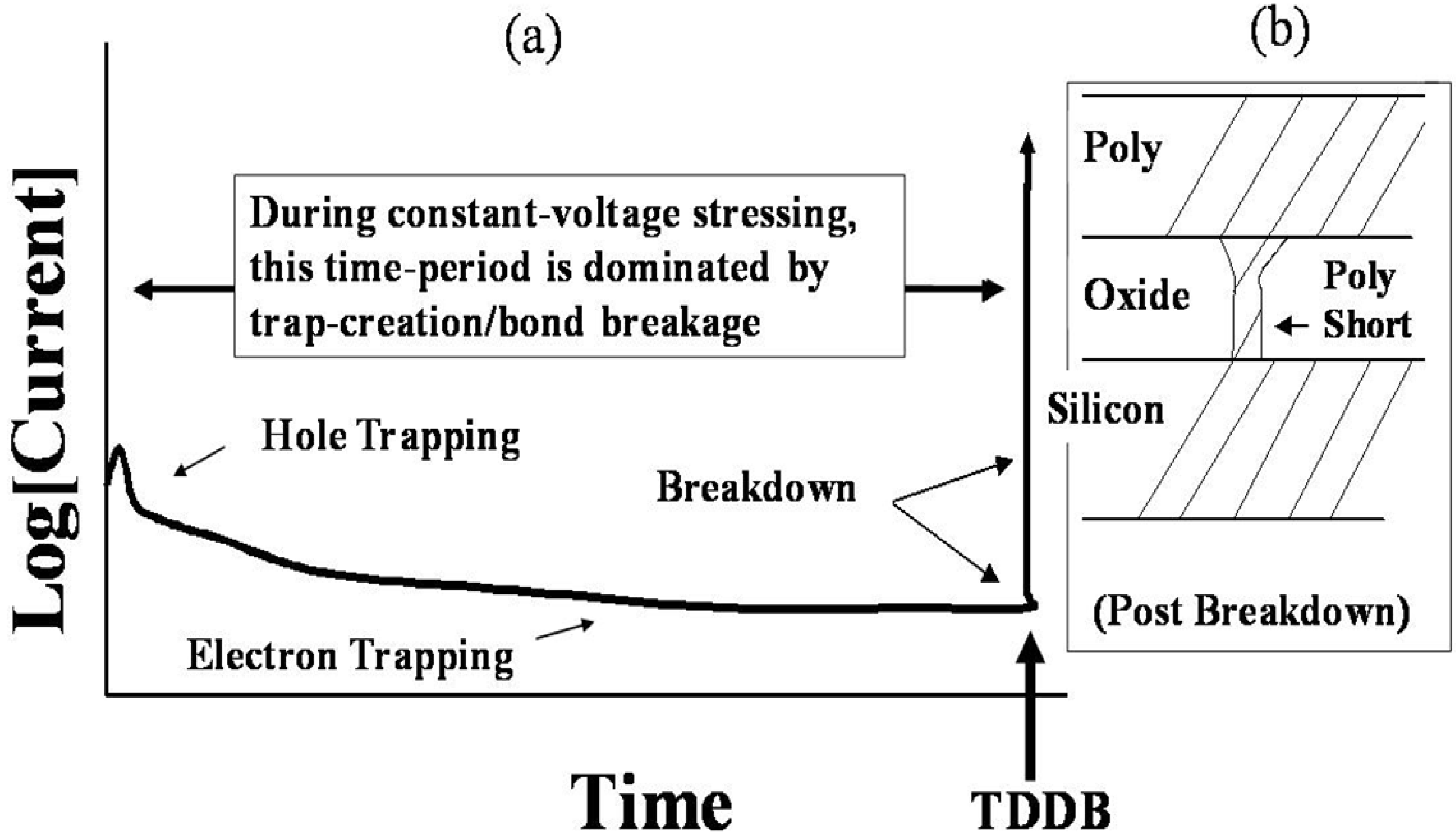
Vgs (V)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	#	27	28	29	30	31	32	33	34	35	36	Vgs (V)
5.0	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟦	🟦	🟦	🟦	🟦	🟧	🟧	🟧	🟧	🟧	🟧	🟧	🟧	🟧	🟥	🟥	🟥	🟥	5.0
4.0	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟦	🟦	🟦	🟦	🟧	🟧	🟧	🟧	🟧	🟧	🟥	🟥	🟥	🟥	🟥	🟥	🟪	🟪	🟪	🟪	🟪	🟪	4.0
2.5	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟧	🟧	🟧	🟧	🟧	🟧	🟧	🟥	🟥	🟥	🟥	2.5
1.0	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟦	🟦	🟦	🟦	🟦	🟦	🟧	🟧	🟧	🟧	🟧	🟧	🟧	🟥	1.0

Vds (V)

Note: Keep-out regions (or very low-duty cycle regions) are clearly highlighted in the HCI-SOA

R-SOA

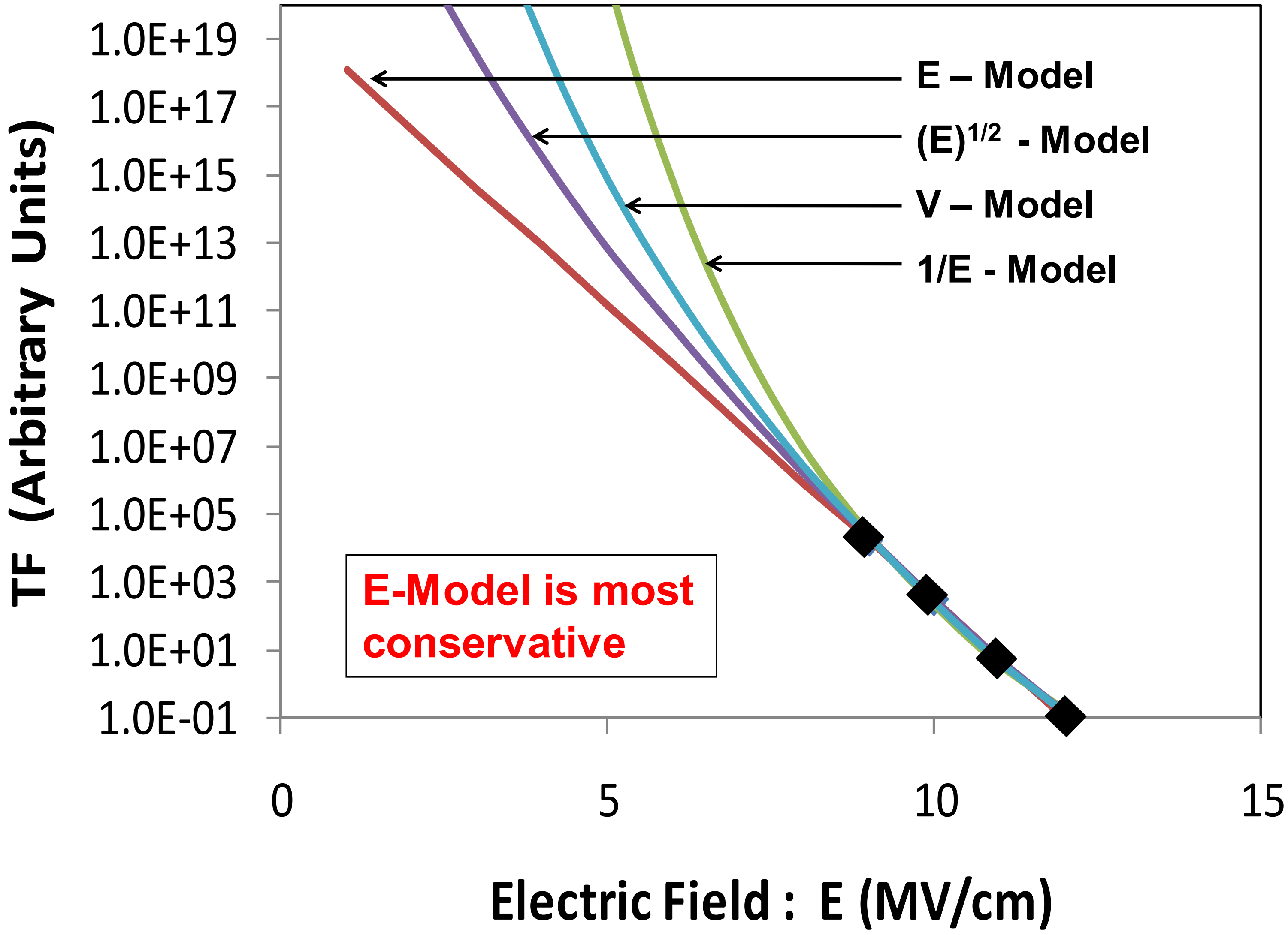
Time-Dependent Dielectric Breakdown



Note: All dielectrics will eventually breakdown

R-SOA

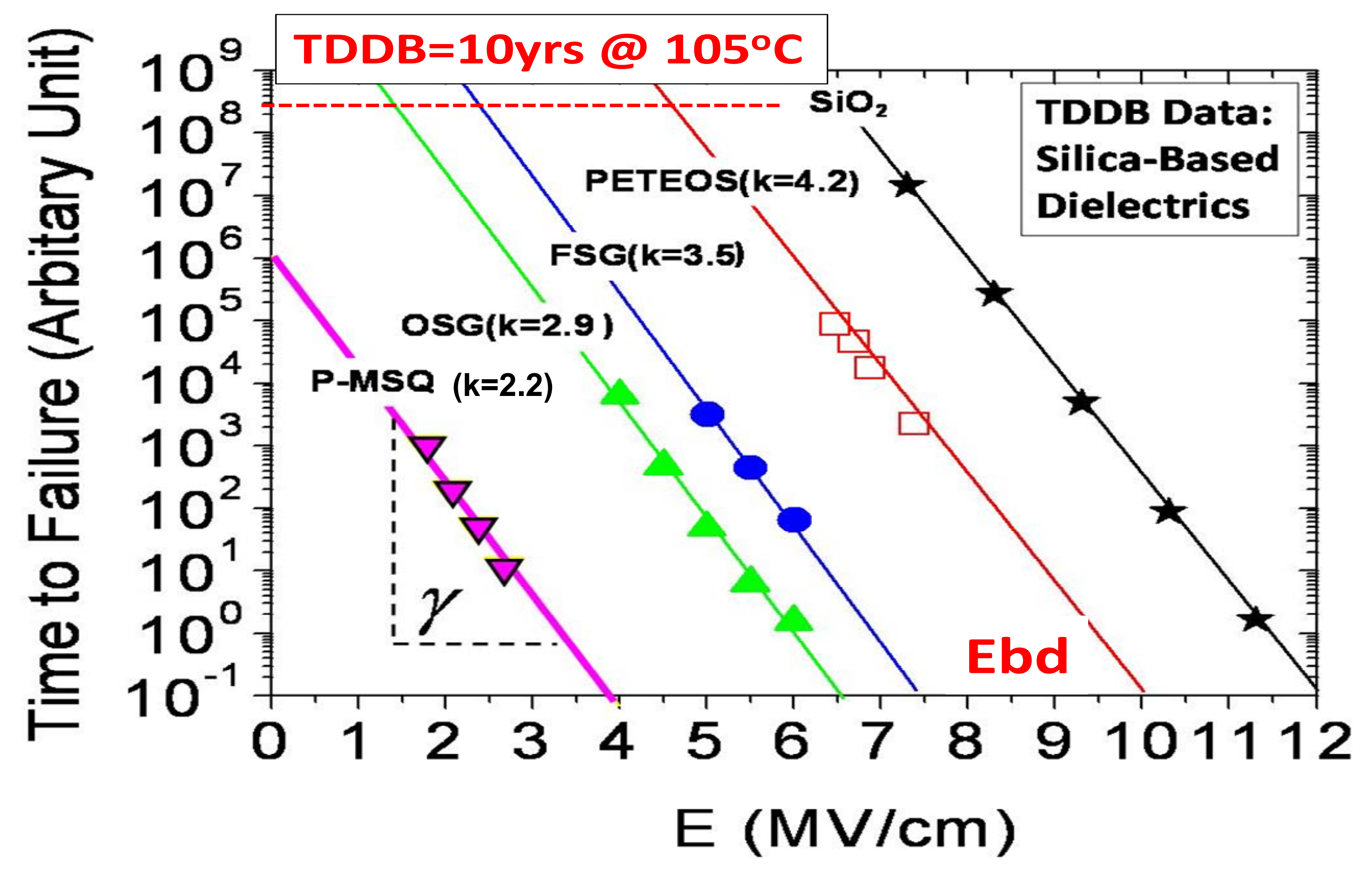
Time-Dependent Dielectric Breakdown Models



E-Model is most conservative

R-SOA

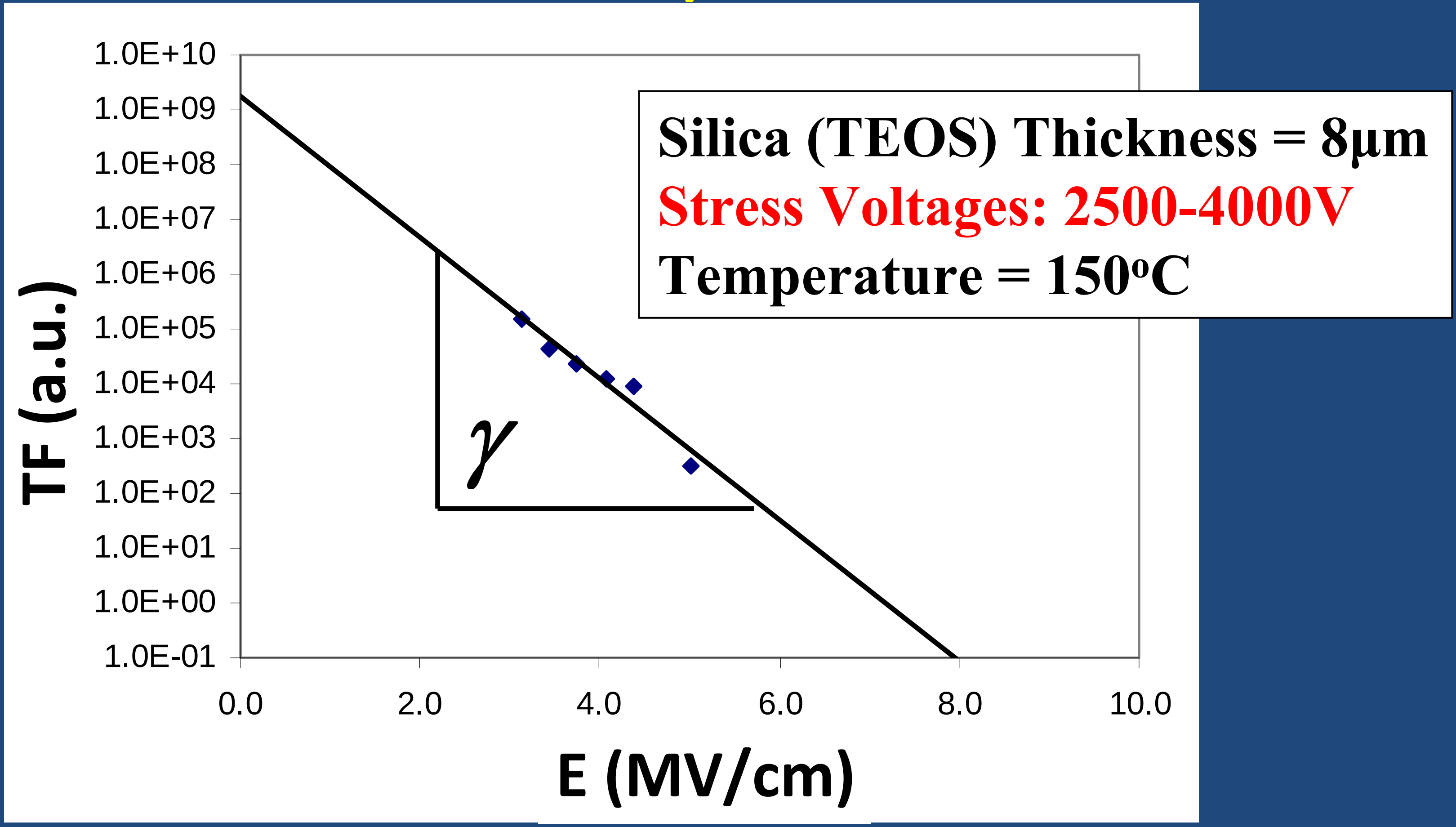
TDDB Data for Silica-Based Dielectrics



Breakdown Strength E_{bd} changes but not slope γ

HV TDDB Data for Silica-Based Dielectrics

HV Isolation Capacitors



Observed: $\gamma(150^{o}C) = 3.22\,cm/MV\ \ (\,for\ \ 8um - Stack)$

- HV TDDB Data (γ) Consistent with LV TDDB.
- No change in TDDB physics at high voltage.

R-SOA

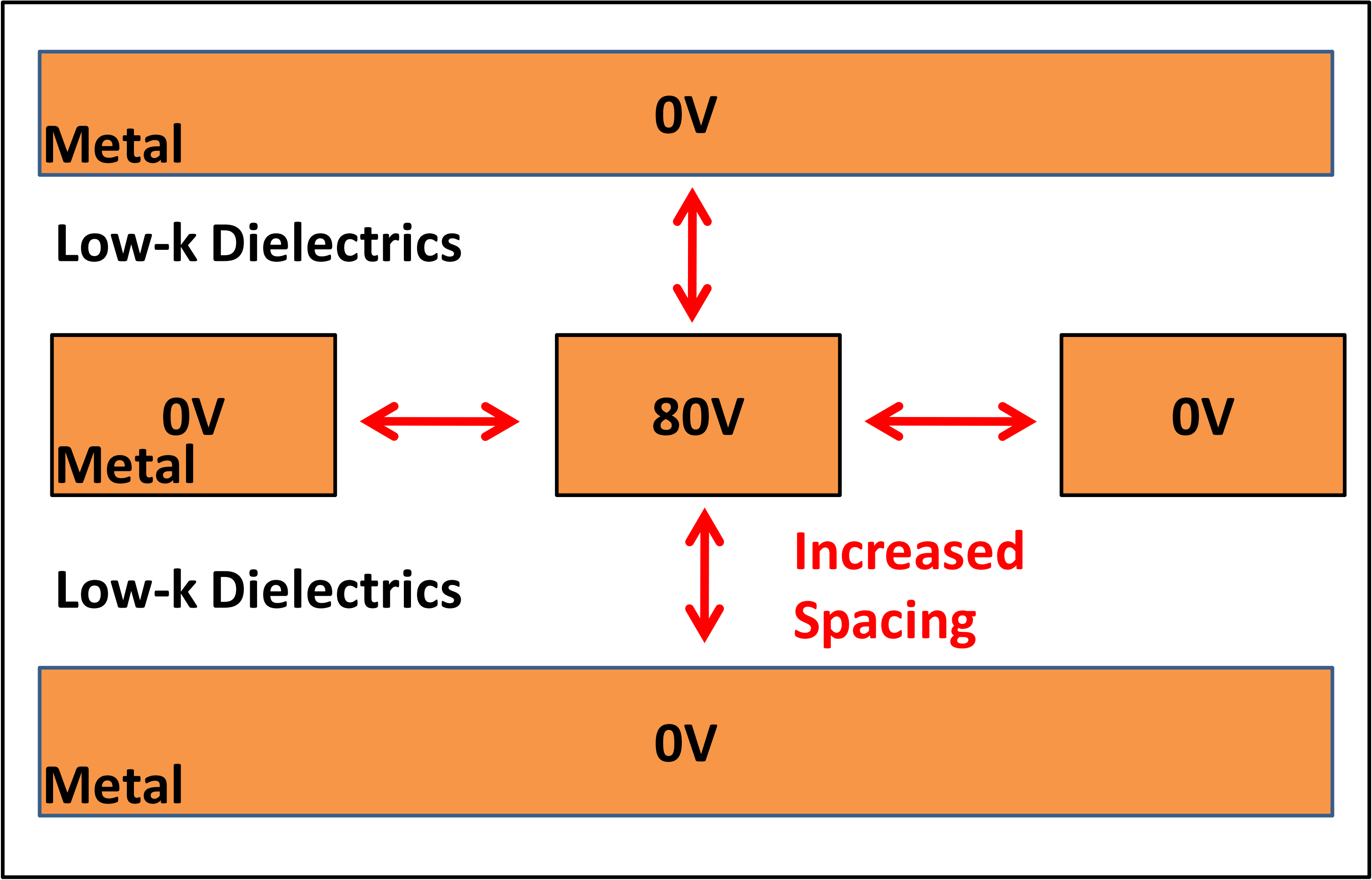
TDDB-SOA for Gate Oxides

Gate Oxide Thickness (Angstrom)	Reference Area (cm^2)	Reference Temp (^oC)	Reference Lifetime (Hr)	Reference Average Failure Rate (Fit)	Reference Field (MV/cm)	Reference Weibull Slope: β	Reference Field Acceleration Parameter: γ (cm/MV)
130 - 200	0.1	105	1.0E+05	10	4	3.0	4.0
50 - 129	0.1	105	1.0E+05	10	5	2.2	4.0
30 - 49	0.1	105	1.0E+05	10	6	2.0	3.6
20 - 29	0.1	105	1.0E+05	10	7	1.5	3.6
12 - 19	0.1	105	1.0E+05	10	7	1.2	3.3

$$AF = \left[\frac{dcyc}{(dcyc)_{ref}}\right] \bullet \left[\frac{Area}{(Area)_{ref}}\right]^{1/\beta} \bullet \exp[\gamma(E_{ox} - (E_{ox})_{ref})]$$

Note: Assumes Good Quality Gate Oxide

DEMOS/LDMOS Interconnect TDDB-SOA



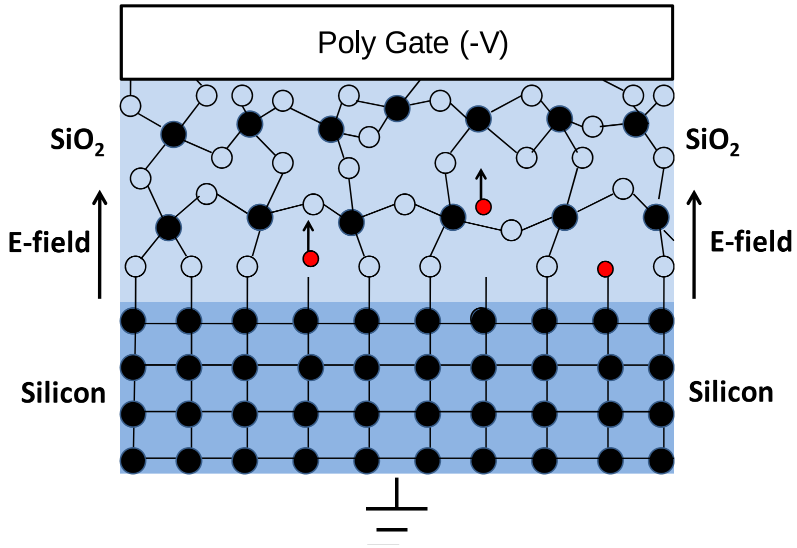
TDDB-SOA (Interconnect Spacing):

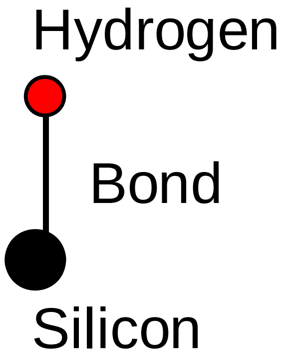
$$(\text{Space})_{\text{min}} = 80\text{V}/(\text{Ebd} - 5\text{MV/cm})$$

NBTI-SOA

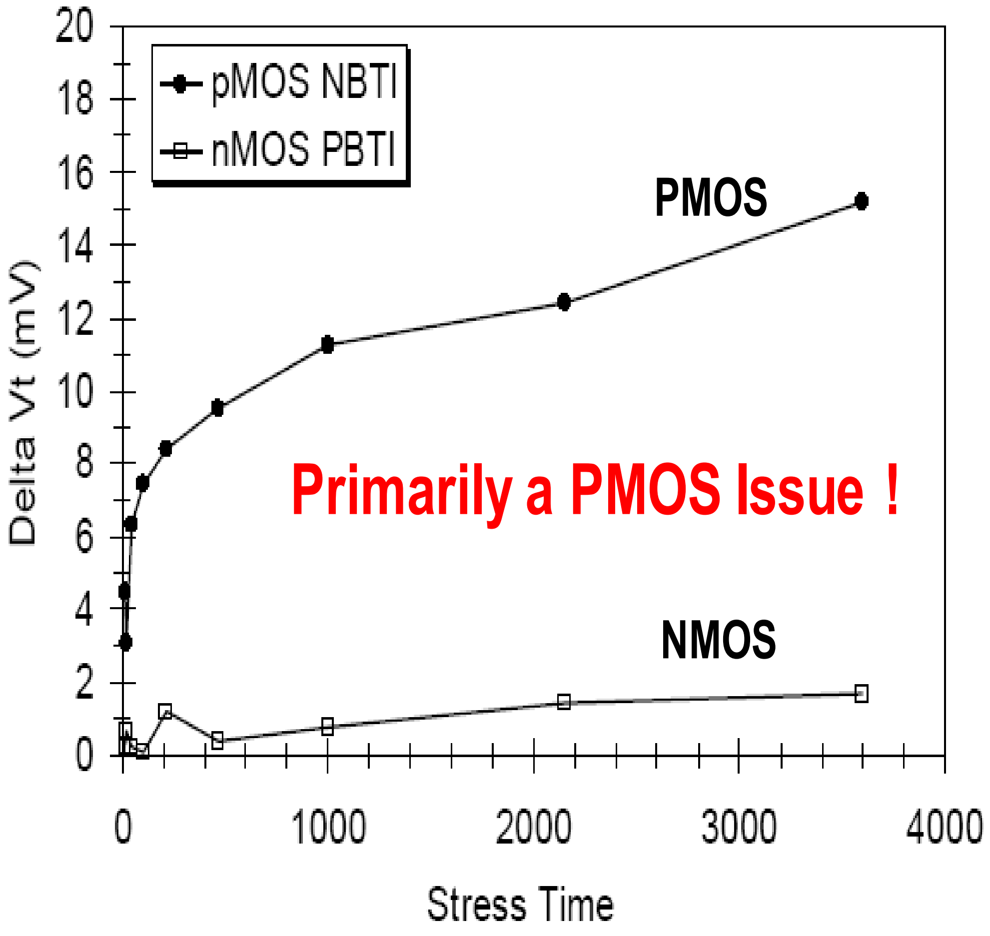
Negative Bias Temperature Instability

P-MOSFET ISSUE





Si-H Bond Breakage will occur causing interface state generation --- Vtp shift

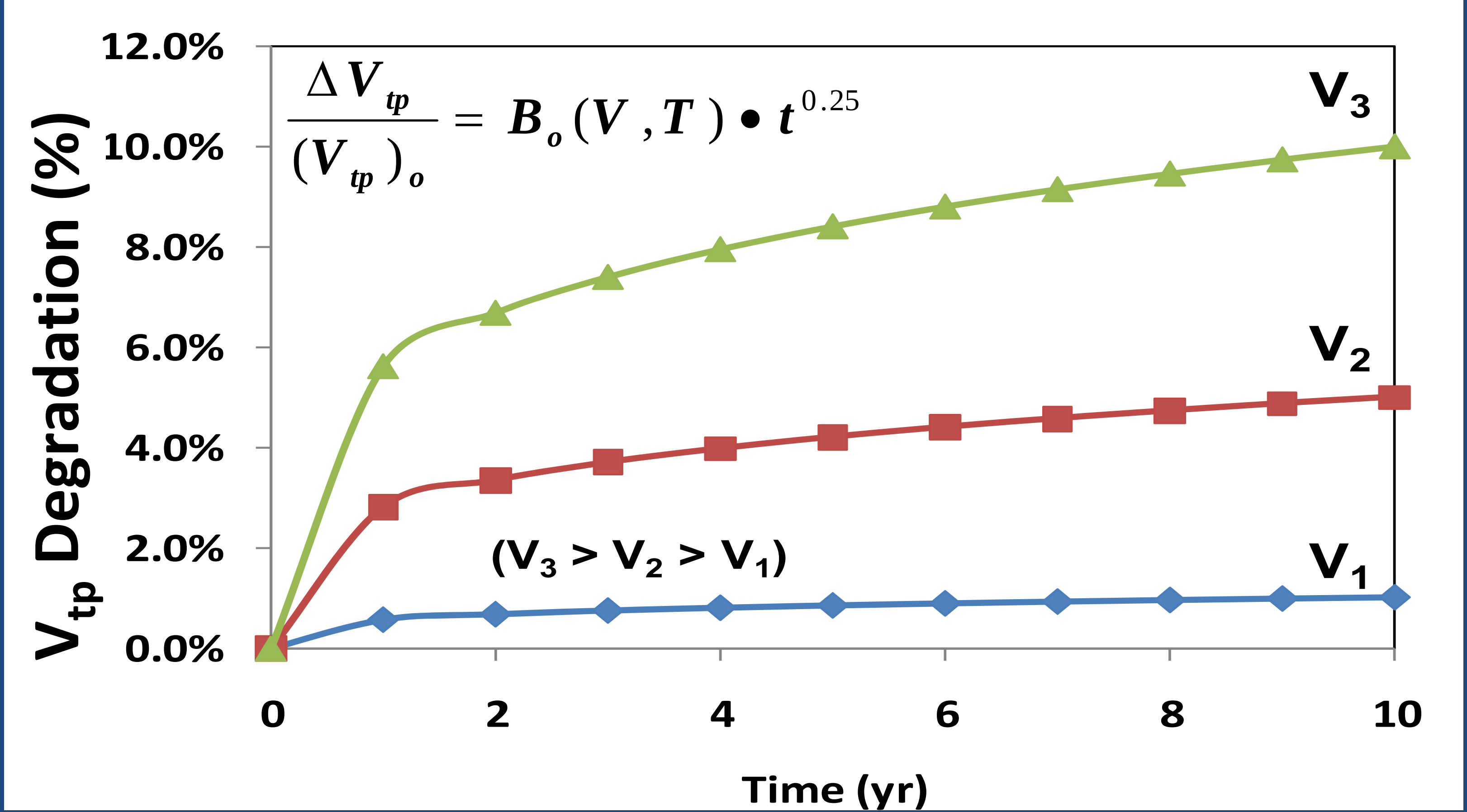


Primarily a PMOS Issue !

NBTI-induced V_{tp} shift caused by Si-H bond breakage

NBTI-SOA

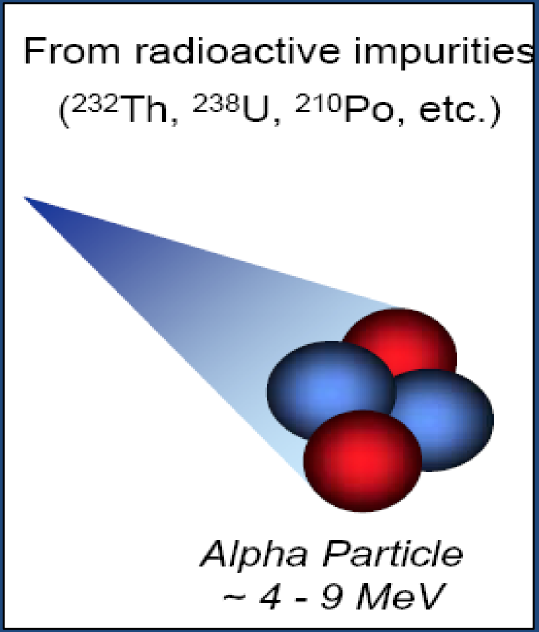
NBTI-Induced V_{tp} Degradation



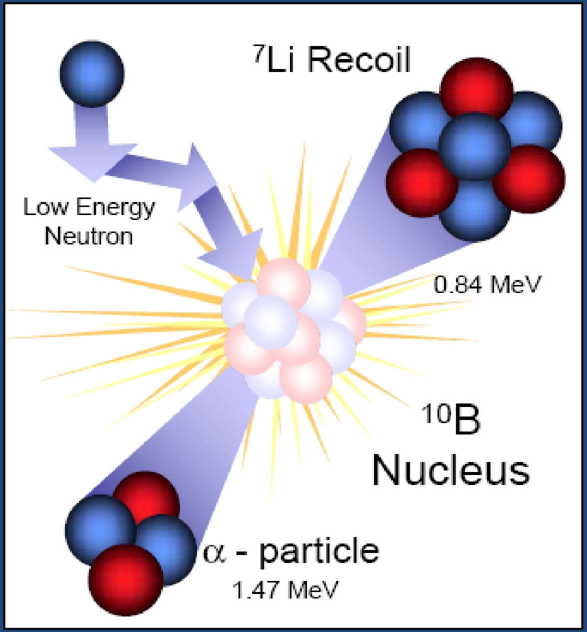
- Most of shift occurs within 1st year of normal product use
- Can be accelerated to a few hours during HTOL for quick evaluation
- NBTI-SOA is presently handled by guard-banding at product level

Single Event Upset (SEU)

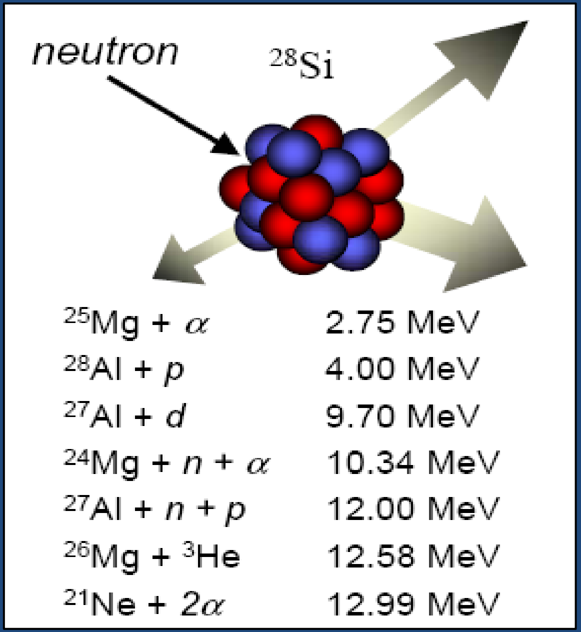
Alpha-Particles



Thermal Neutrons



High-Energy Neutrons



^{25}Mg + α	2.75 MeV
^{28}Al + p	4.00 MeV
^{27}Al + d	9.70 MeV
^{24}Mg + n + α	10.34 MeV
^{27}Al + n + p	12.00 MeV
^{26}Mg + ^{3}He	12.58 MeV
^{21}Ne + 2α	12.99 MeV

Important Reliability Considerations for SEU:

- Materials selection which are low in radioactive impurities
- Removal of ^{10}B from BPSG process
- SER calculator/simulator
- Error correction
- Layouts to reduce multiple-bit errors
- SEU Induced Latch-up

SEU Impact on HV Devices:

---Hard failures due to SEU induced latch-up

--- Hard Failures due to TDDB in High-Voltage Capacitors

Conclusions

☐ The business demand for HV components is great

☐ HV components, such as DEMOS and LDMOS devices, can be safely integrated with LV CMOS when careful attention is given to Safe Operating Areas:

--- e-SOA
--- T-SOA
--- R-SOA

☐ SEU-induced hard failures will need to be investigated more closely for HV devices