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Analog Yield Optimization

October 16, 2009

Outline: Analog Yield Optimization

- Key Factors in Analog IC Technology
- Methods to Characterize Variation
- Methods to Optimize Circuit Performance
- Fault Detection and Control to Control Variation

A Sample of Dongbu HiTek's Analog Portfolio

Technology Node	Product Function	Total Chip Area	% of Chip Area		
			Logic	Memory (eg, OTP, NVM)	Analog
BD350	LED driver IC	2345x2345	23%	0%	77%
	LED driver IC	2938x2938	28%	2.5%	69.5%
	PMIC for TV	3828x3681	1.5%	2.5%	96%
	PMIC for N/B	3169x3170	1.5%	2.0%	96.5%
	Inverter for CCFL	1865x1865	0.5%	0%	99.5%
	RF Barcode	4120x3775	87%	0%	13%
	Solar Industry	2900x2850	1.5%	0%	100%
	Class D Audio Amp	1420x1650	2.5%	0%	97.5%
BD180	LED Driver	2600x3400	17%	0%	83%
	Piezo Driver	2000x1000	33%	0%	67%
	Switch Mode Power Supply	870x1100	0%	0%	100%
	Level Shifter	1460x1460	0%	0%	100%

Analog Yield Optimization: Problem Statement

- **Analog Products uniquely designed to fit the application**
  - Analog / Digital Area Partition is quite diverse
  - Single Chip solutions still thought to be best for low power / end-user package space
- **Analog Components to interface to real world sensors**
  - High Voltage Transistors
  - Precision capacitance & Resistance
  - Precision transistors to minimize offset voltage
- **Advanced node CMOS used to**
  - Enable digital signal processing to replace some analog circuitry
  - Meet Digital Interface speed / voltage requirements
- **Memory components sometimes needed for trim and calibration**

- **No Analog Yield Penalty Allowed**
- **Advanced CMOS costs make Analog "real estate" expensive**

Key Factors & Strategy for Analog Products

- **High Tolerance Specifications and Accurate Models**
  - Cost Advantage from reduced Die Area
  - Requires Extremely Efficient Characterization in Technology Development
    - Layout Attribute device Dependencies
    - Systematic Process and Lithographic issues with Flow Integration

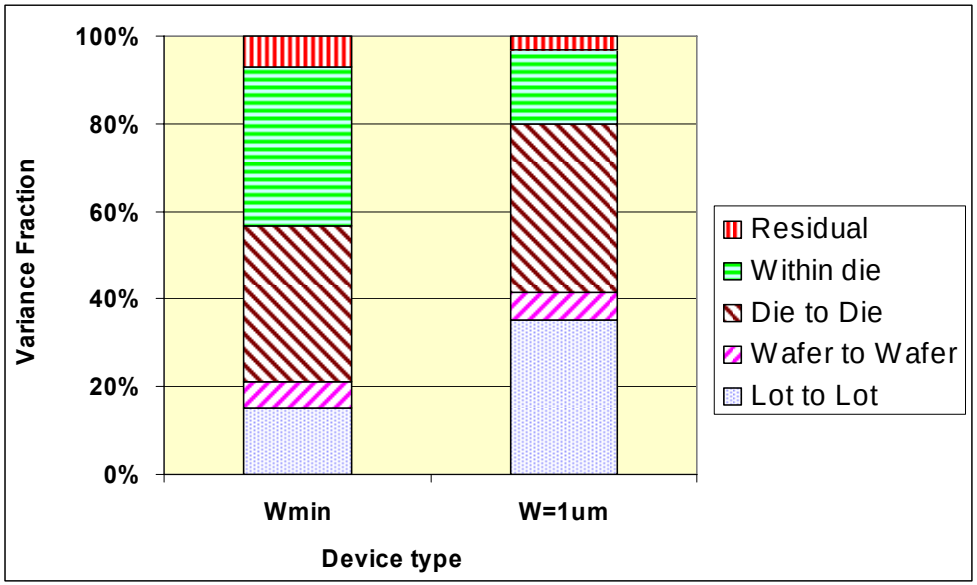
- **Reliable Production**
  - Cost Advantage from Higher Yields
  - Requires Increasing Tool Level Knowledge, Tool Matching, and Monitoring

- **Minimize Shifts due to Stress in the Field**
  - Customer Satisfaction from Highly Reliable Products
  - Maintain Process stability & conformance to original qualification process distributions

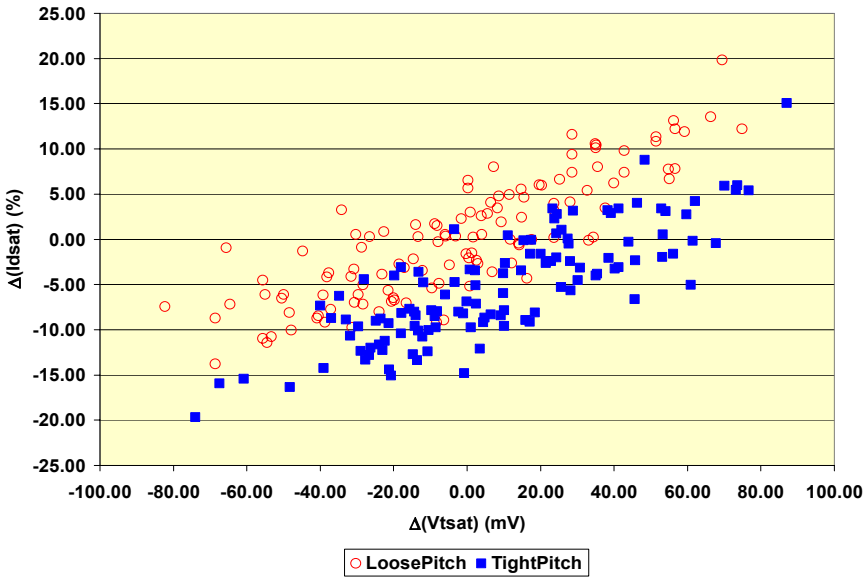
- **Characterization of Device Variation (and the sources)**
- **Minimize Variation through Layout**
- **Minimize Variation in Fabrication**

Sources of variation

Decomposition of random variation

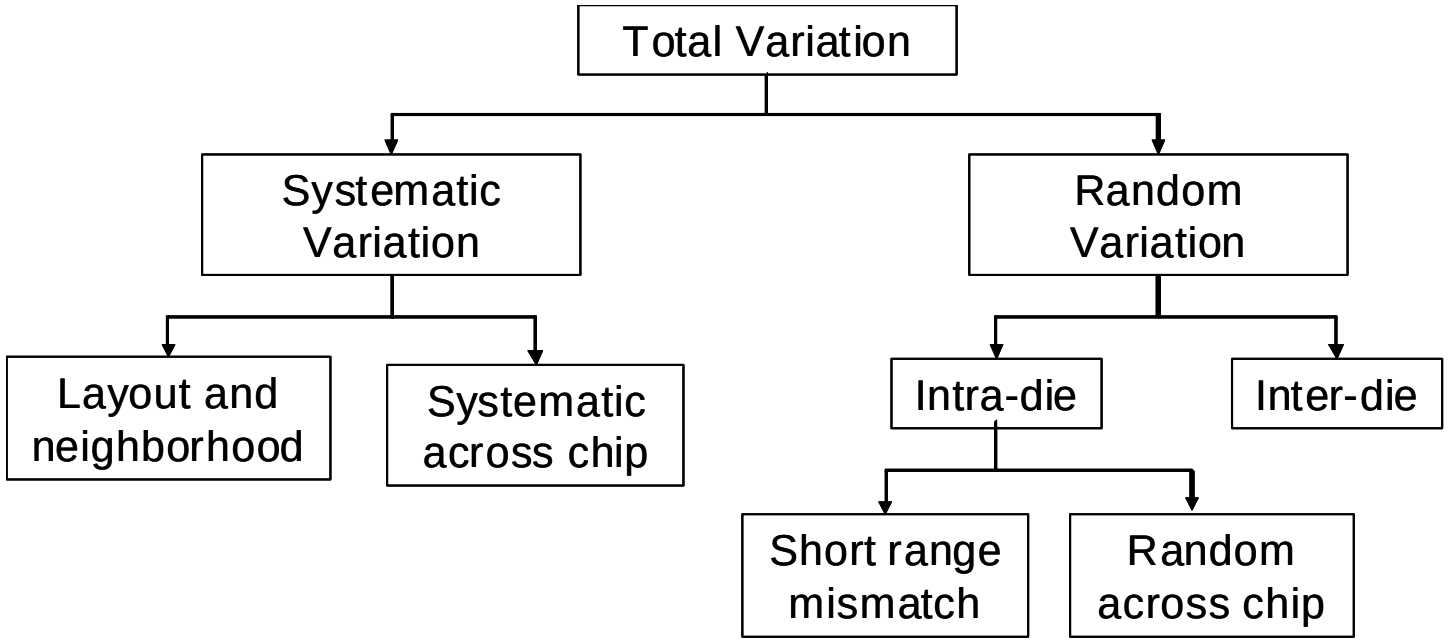


Variation from layout effects



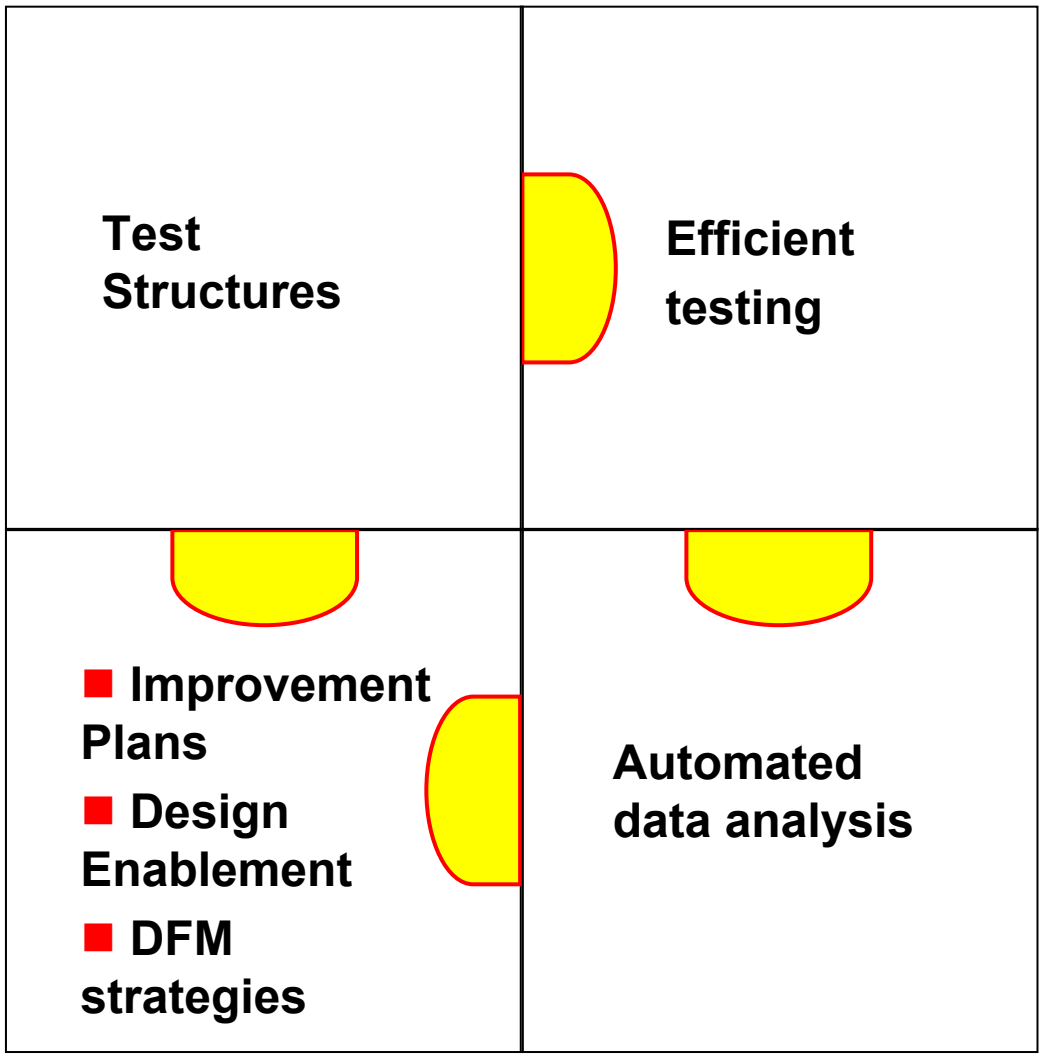
- Many different sources of variation
- Minimizing variability and mitigating its impact requires accurate and efficient characterization of all sources of variation

Classification of Variance



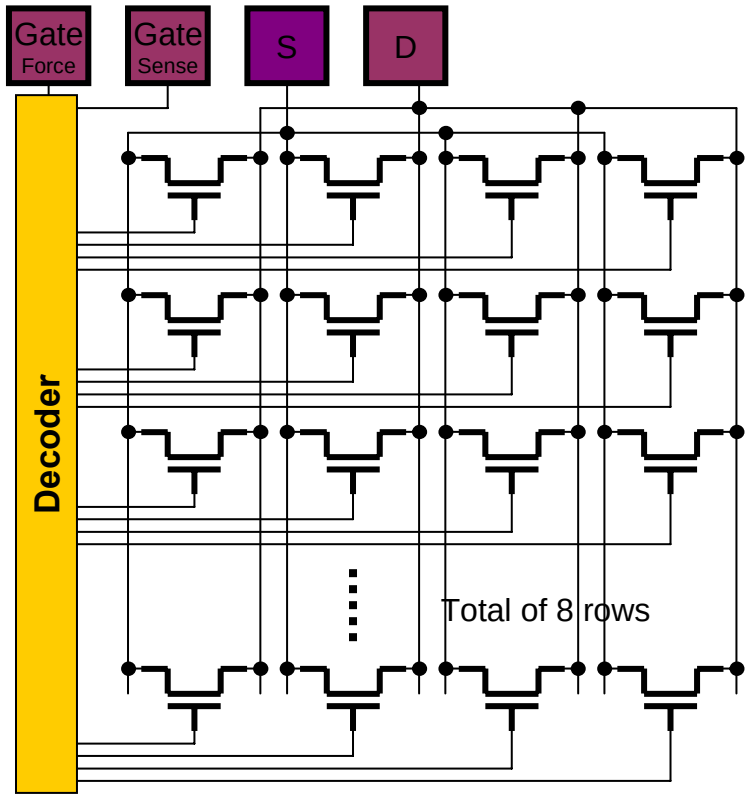
- **Random: variation in characteristics of devices with identical layout and neighborhood**
  - Random Dopant Fluctuations, LER, Across-chip variation, die-to-die variation
- **Systematic: variation in characteristics of devices with identical dimensions (W, L)**
  - Layout and neighborhood effects, deterministic process gradients

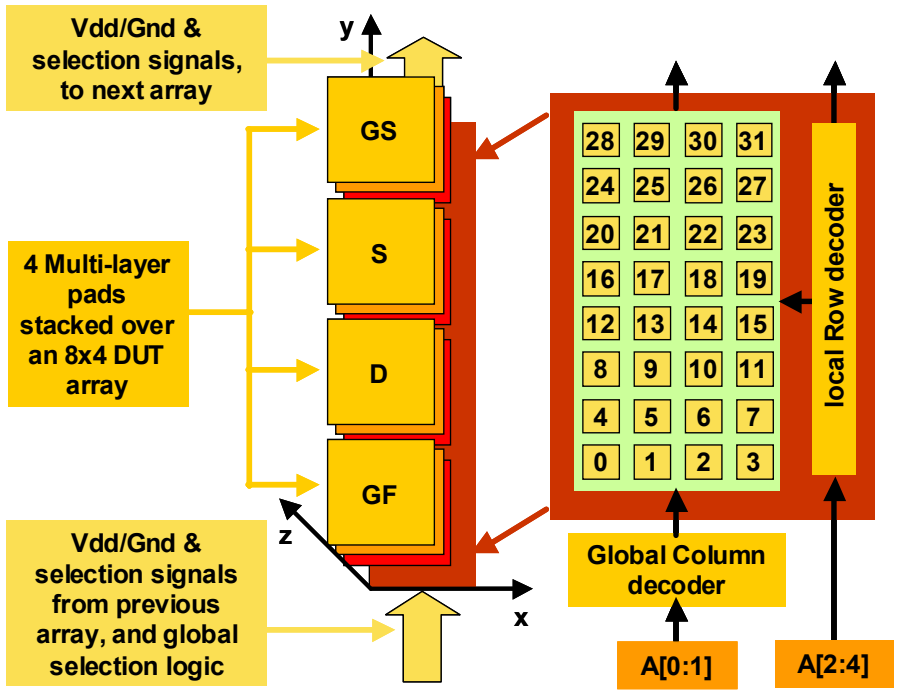
Infrastructure to Characterize Variation Effectively



- **Integrated Infrastructure:**
  - Generate
  - Test
  - Manage& analyze
  - Model and apply characterization data

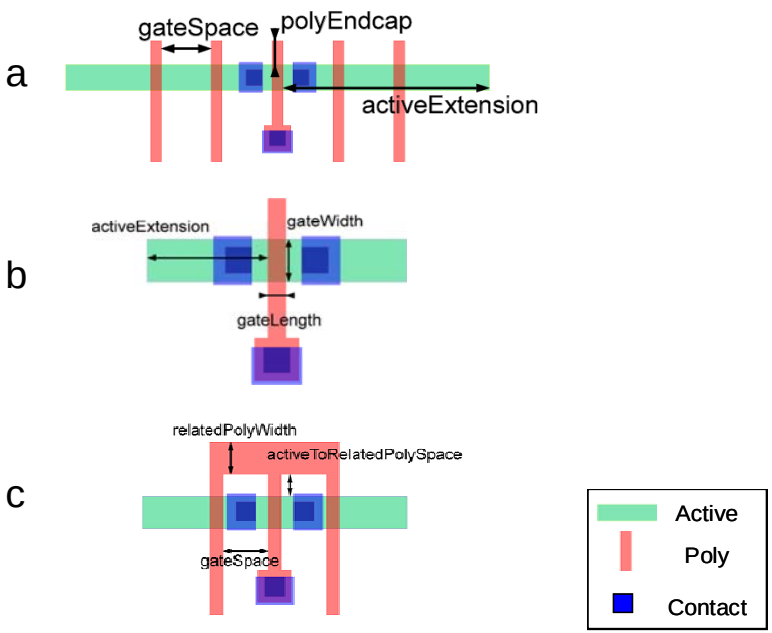
Test Structures (1)

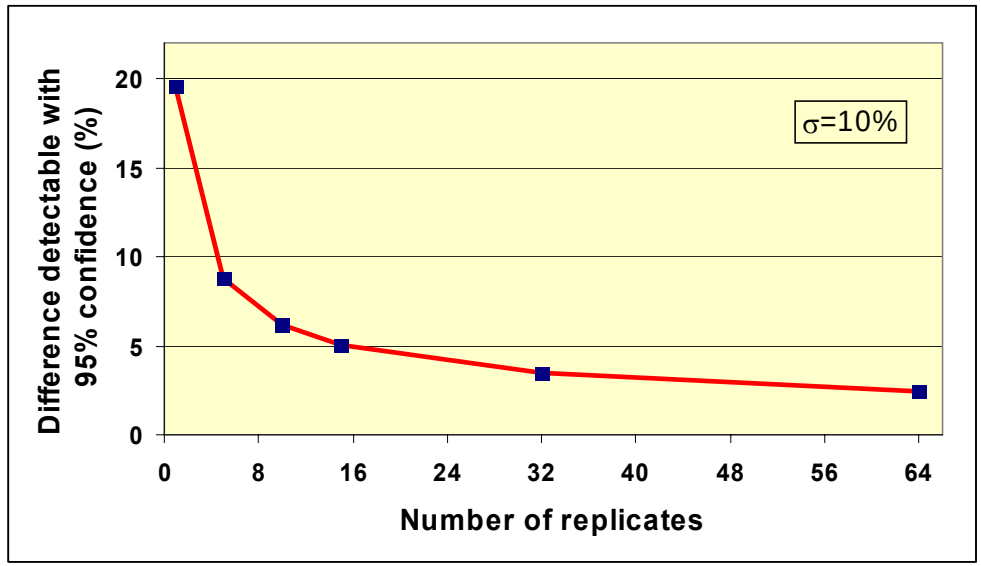




- **Multiplexed arrays provide pad-efficient test-structures**
  - Large number of replicates or layout experiments
- **Array can be placed below pads for even more area-efficiency**
  - Scribe-line applications

Test Structures (2): Experiments

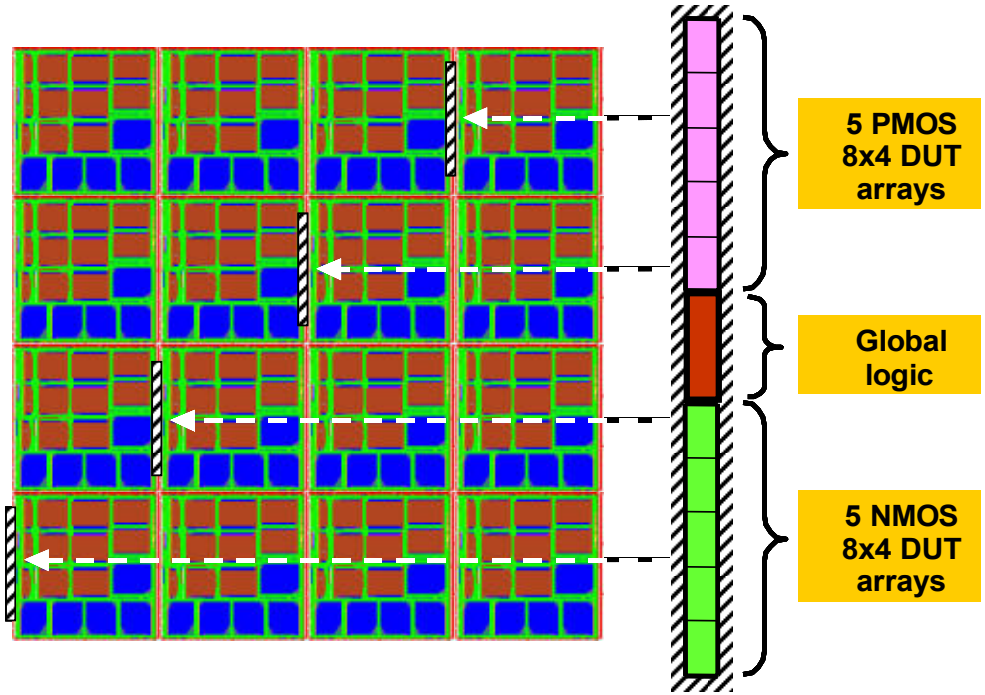


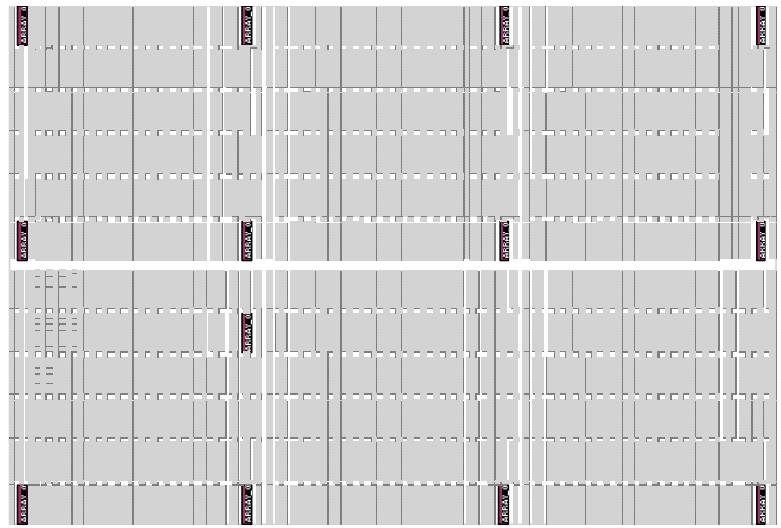


- **Different sizes, layout styles and neighborhood**
- **Characterize systematic variability from layout**

- **Large number of replicates**
  - Detect systematic differences in presence of variability
  - Variance decomposition

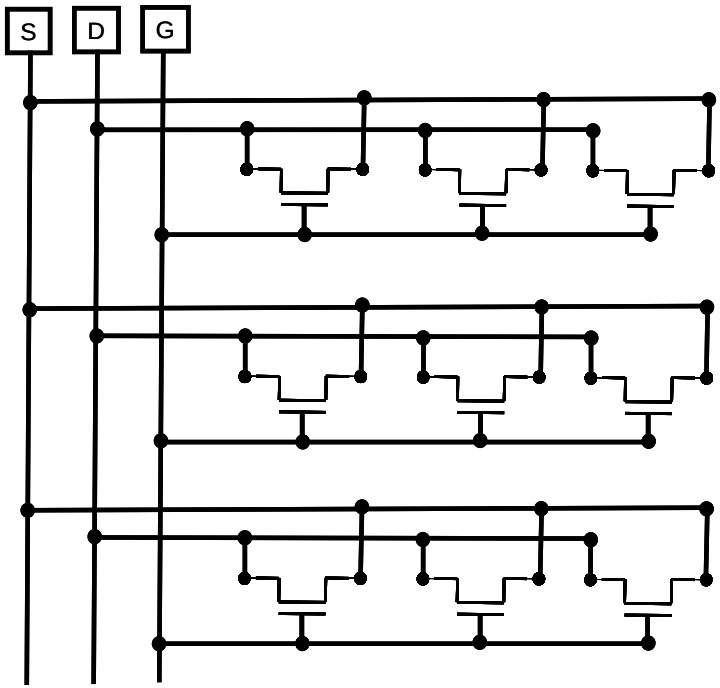
Test Structures (3): Placement





- **Scribe-line placement on products**
  - Yield ramp and production monitoring
- **Across-chip placement**
  - ACV effects
  - Technology development and characterization

Leakage Structures (4): Leakage Arrays



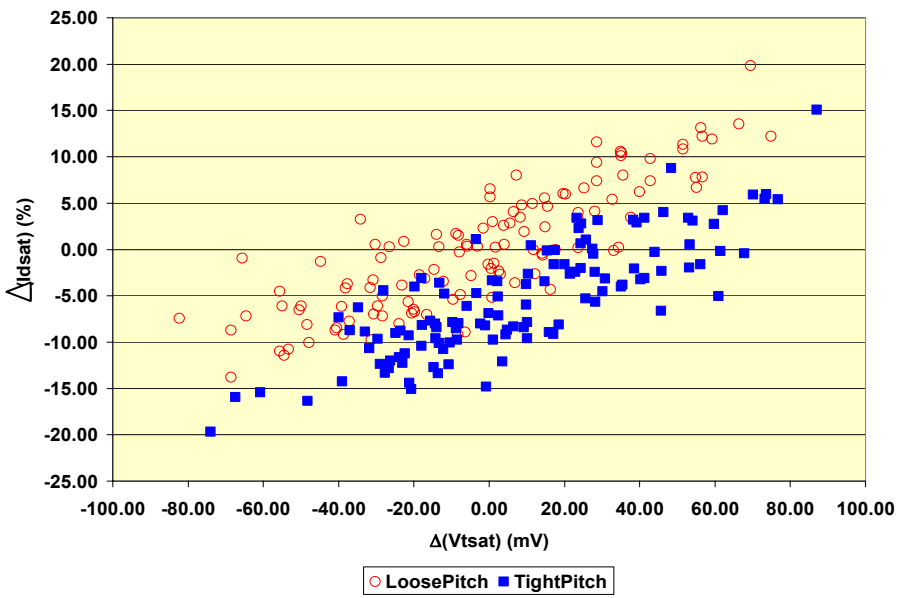
- **Leakage structures each containing 100's of devices**
  - Many parallel devices in each DUT for fast testing (higher current → less settlement time) and suppress impact of local mismatch
- **Each structure has independent S/D/G/W**
- **Large number of parallel structures for leakage characterization**
  - Experiments on layout and neighborhood
- **Many leakage paths**
  - All need to be characterized and understood
  - Trade-off between leakage and variability

Fast Testing

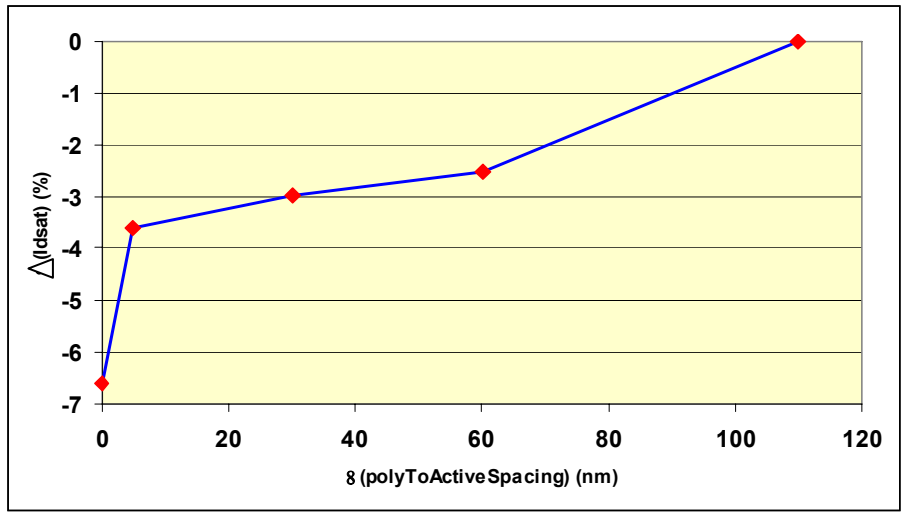
- Variability characterization ➔ large sample sizes, multiple placement, many experiments
- How can all the measurements be made in reasonable time?
- Parallel testing: many devices at the same time
- Low-resolution “inexpensive” measurement units

Applications: Systematic variation

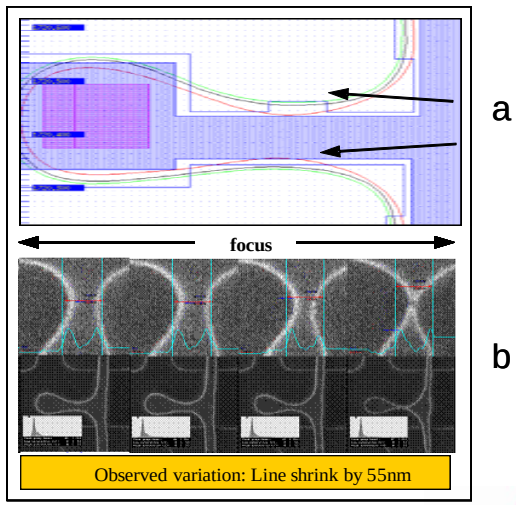
Gate pitch



Gate corner rounding



- **Infrastructure enables:**
  - a. Characterization of layout effects
  - b. Characterization of process window

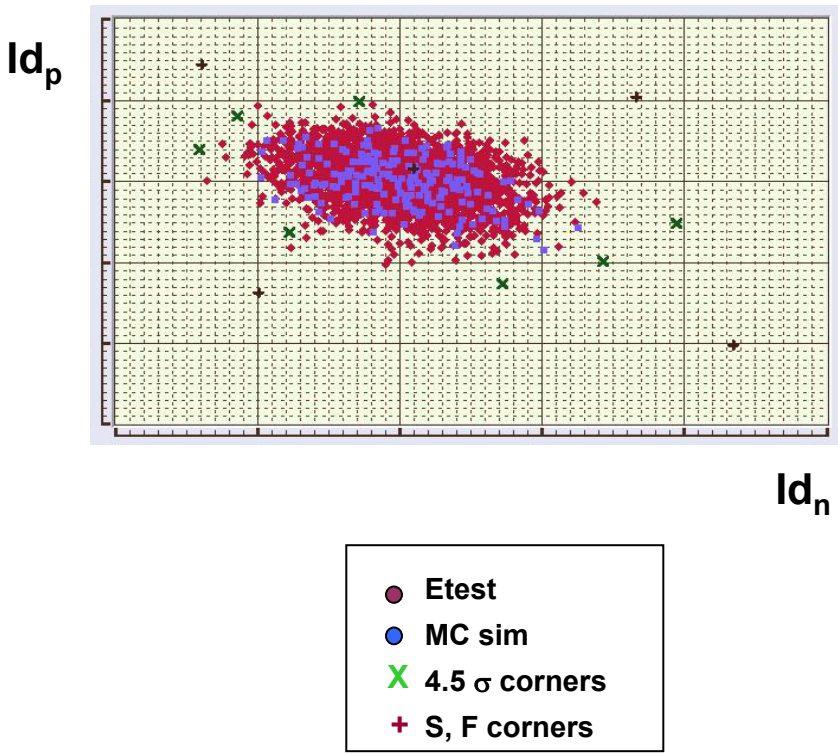


Systematic variation: Sample phenomena

Layout effect	Typical impact at 65 nm
Poly pitch: printability	3-5% change between pitches
Poly pitch: stress	5-10% change in Idrive
Poly orientation	2%-7% change in Idrive
Poly local neighborhood; e.g. center vs. edge gate	1-10% difference between center and edge gates (depends on OPC)
Poly corner rounding	2-7% decrease in Idrive for worst case
STI Stress	PMOS Idrive: 5-8% NMOS Idrive: 12-18%
Active corner rounding	1-5% Idrive increase for worst case
Gate counter-doping	6-10% decrease in PMOS Idrive
Contact density	3-5% Idrive decrease between dense and spare contacts

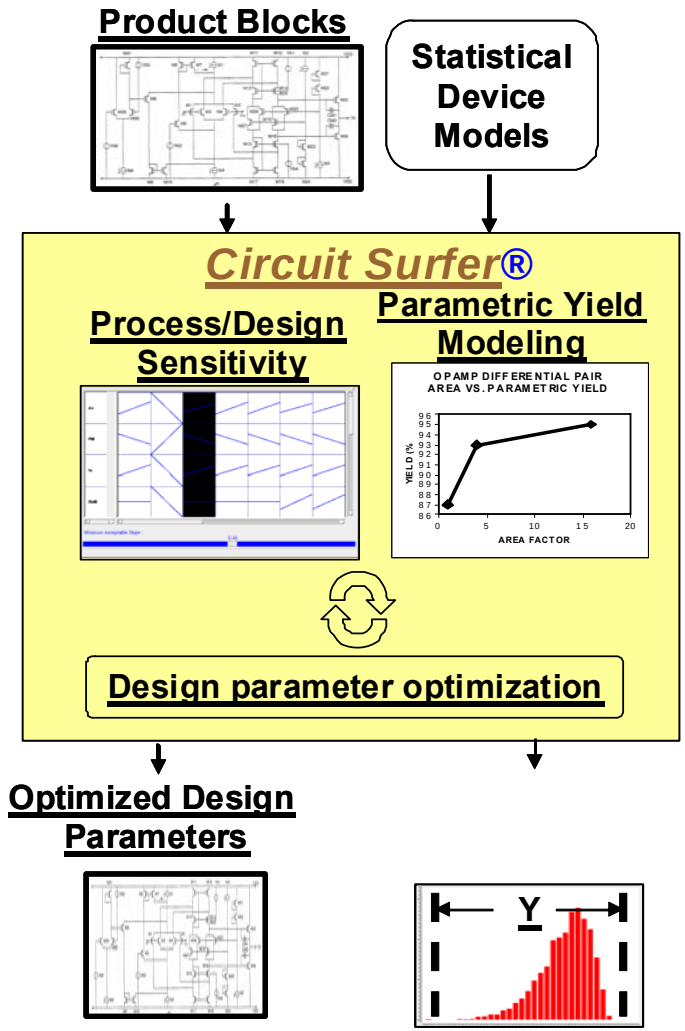
Modeling & Design Enablement

- **Statistical SPICE models**
- **Design tools for transistor level design**
  - Monte-Carlo Simulation
  - Design of experiments
  - Response surface methodology
  - Application-specific worst-case corners
- **SPICE models with switches for layout effects**
- **Statistical static timing analysis (SSTA)**
- **Tools and capabilities continue to be limited**



Block Level Statistical Design Tools and Flows

- **Suitable for: Analog, RF, Standard Cell design, SRAM**
- **Requirements/Features**
  - Monte-Carlo
  - DOE/RSM methodology
  - Efficient mismatch simulation
  - Sensitivity analysis: process and design variables
  - Application specific worst-case corner extraction
- **Results in best case die area**



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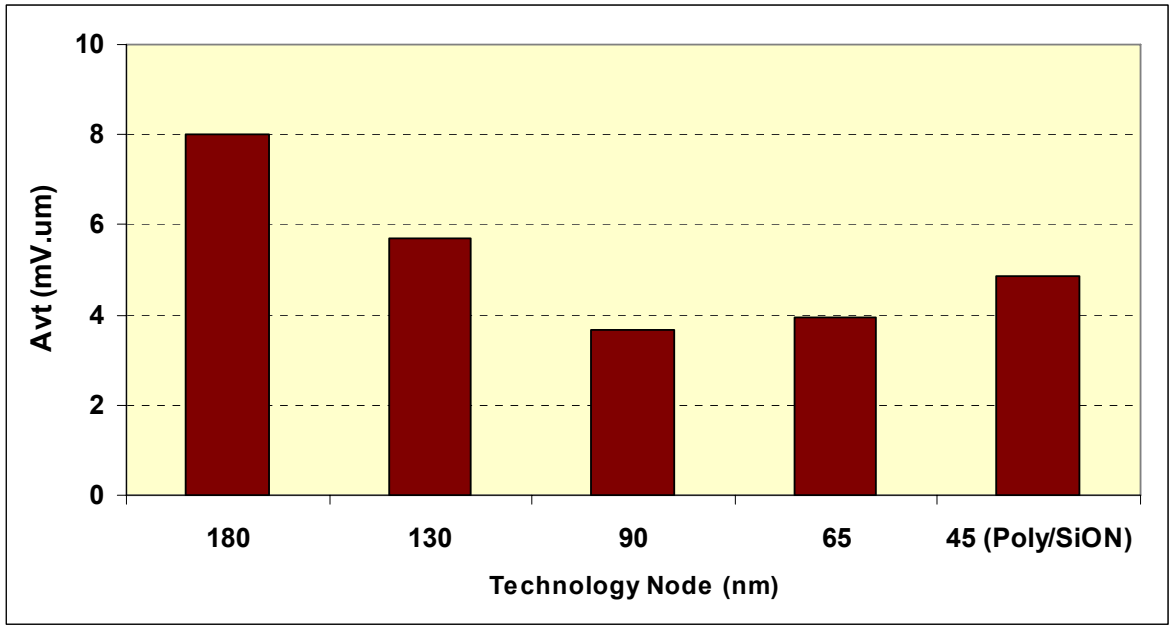
Local Variation Does Not Scale

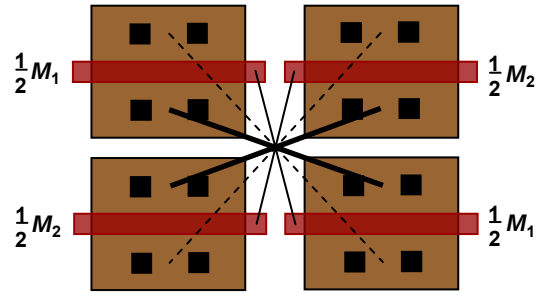


$$\sigma(\Delta(Vth)) = \frac{A_{VT}}{\sqrt{WL}}$$

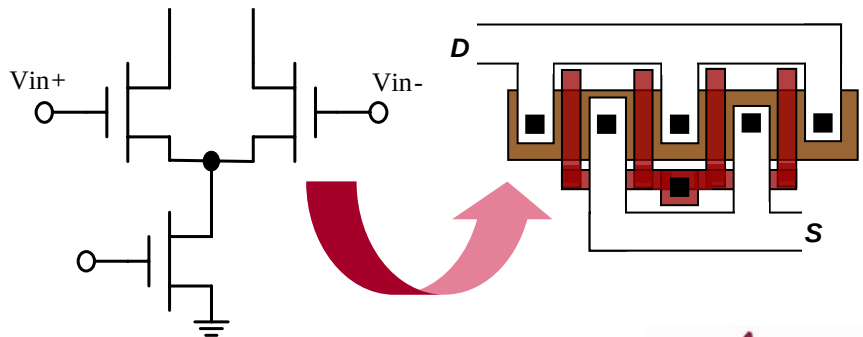
- Lack of T_{ox} scaling with SiON places severe restrictions on local variation (mismatch) improvement
- Efficient infrastructure facilitates technology optimization for local variation minimization

Reduce Variation by Stochastic Analog/RF Design

- **For analog design, regular layout styles have always been applied to control systematic mismatch**
  - Dummy devices
  - Concentric layout styles

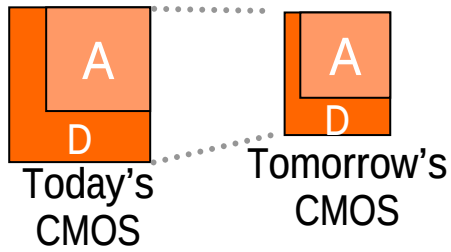


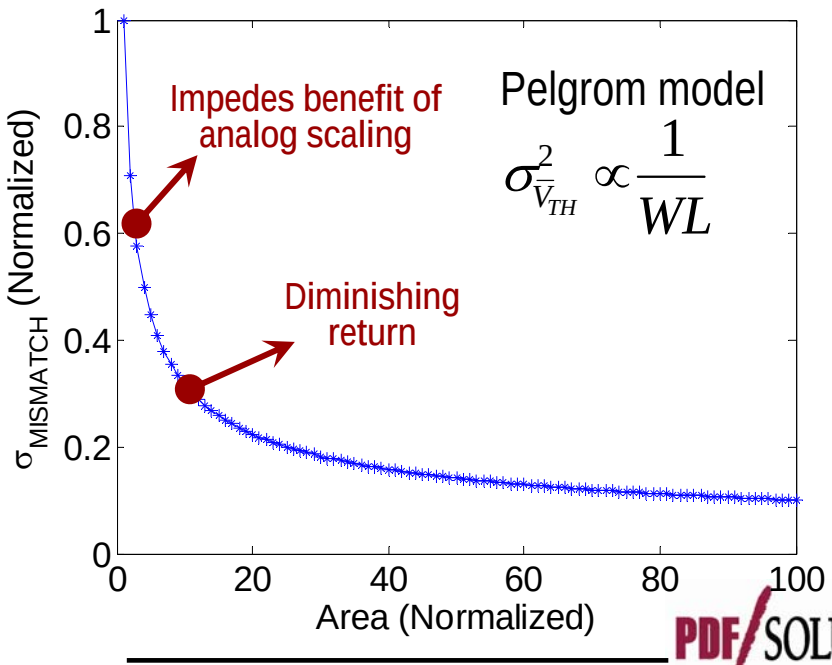
- **Devices are oversized to *average out* random variations**
  - Use enough transistor fingers to reduce the uncertainty to acceptable levels



Analog/RF Design in Scaled "Digital" CMOS

- As CMOS continues to scale, there is a diminishing return with using large devices to average out fluctuations
- Oversizing transistors can potentially cancel any benefit of moving to the next generation technology
- Example: Pelgrom model analysis of a 65nm differential pair
- Mismatch improves slowly with increasing transistor size
  - ~1/sqrt(area)





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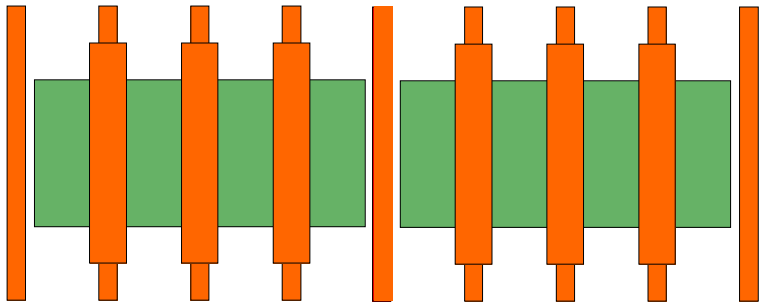
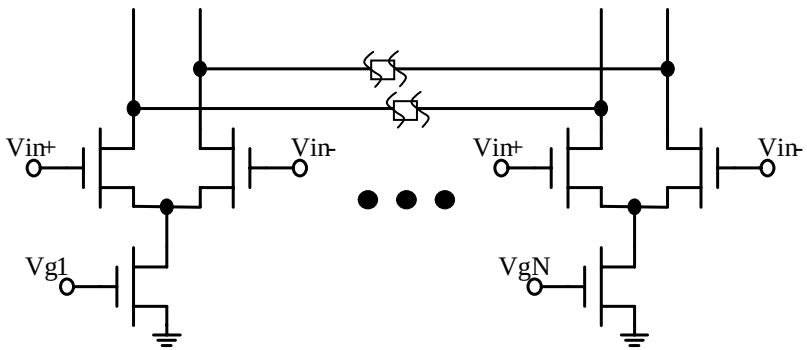
Sizing via Selection of Elements

- Start with regular "fabric" of analog sub-components but "select" only a subset of them for precision matching



- **Ex:** open-loop amp for pipeline ADC mismatch in 65nm CMOS
  - Select *some* (~1/2) rather than *all* subcomponents to minimize offset

w/ Configuration		w/o Configuration	σ_{OS}
# Fingers	W (µm)	W (µm)	
1	1	1	11.8mV
4	4	4.79E+01	1.71mV
8	8	2.74E+03	0.226mV
14	14	4.24E+06	5.75µV



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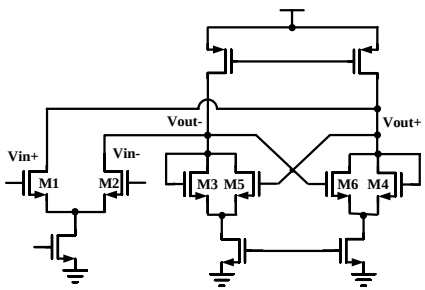
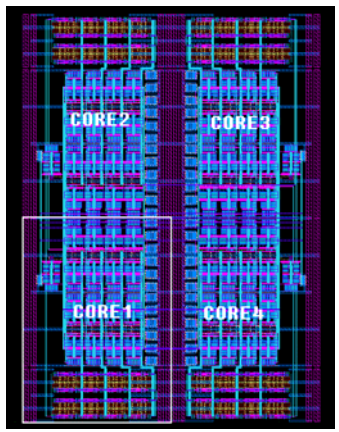
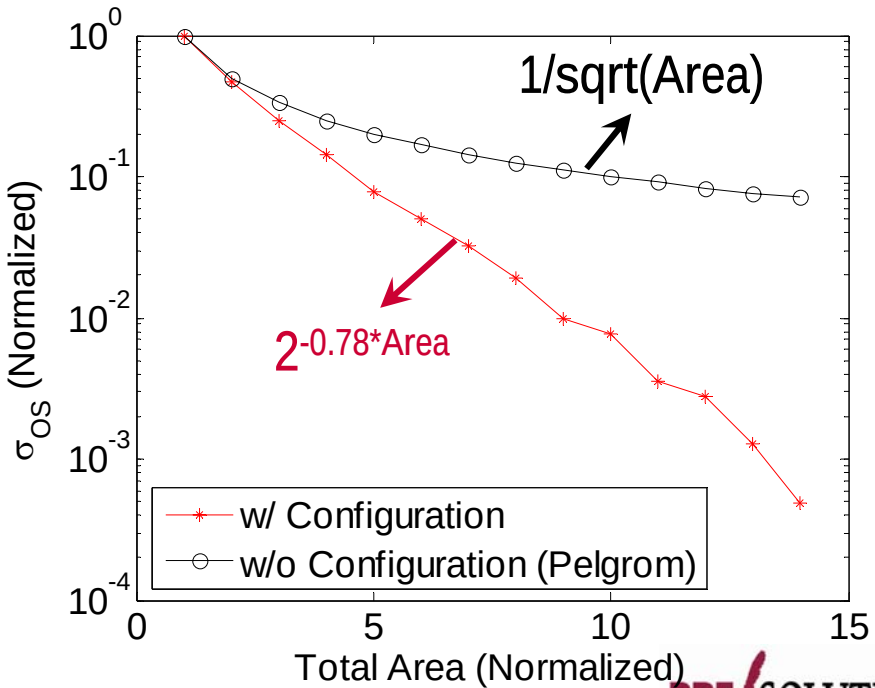
Post-Silicon Element Selection for Mismatch

- **Some circuit overhead required to implement post-silicon tuning**
  - But with further scaling, post-silicon tuning might be the only way to meet specs and reap the benefits of next gen technology
- **Example: Exponential vs. sqrt improvement (Pelgrom model) with area for 65nm open-loop amplifier**







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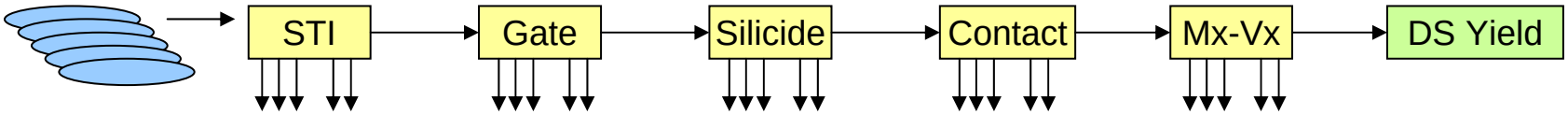
Control Variation in Fab Process by Fault Detection & Classification

Standard (unsupervised) statistical FDC challenge:

- Amount of process signal data in fabs is rapidly increasing
- The more data available, the more likely false alarms



FDC monitoring system
100,000s charts for each module
Over a million SPC charts in a fab !!
High false alarms or drastic detuning of the monitors

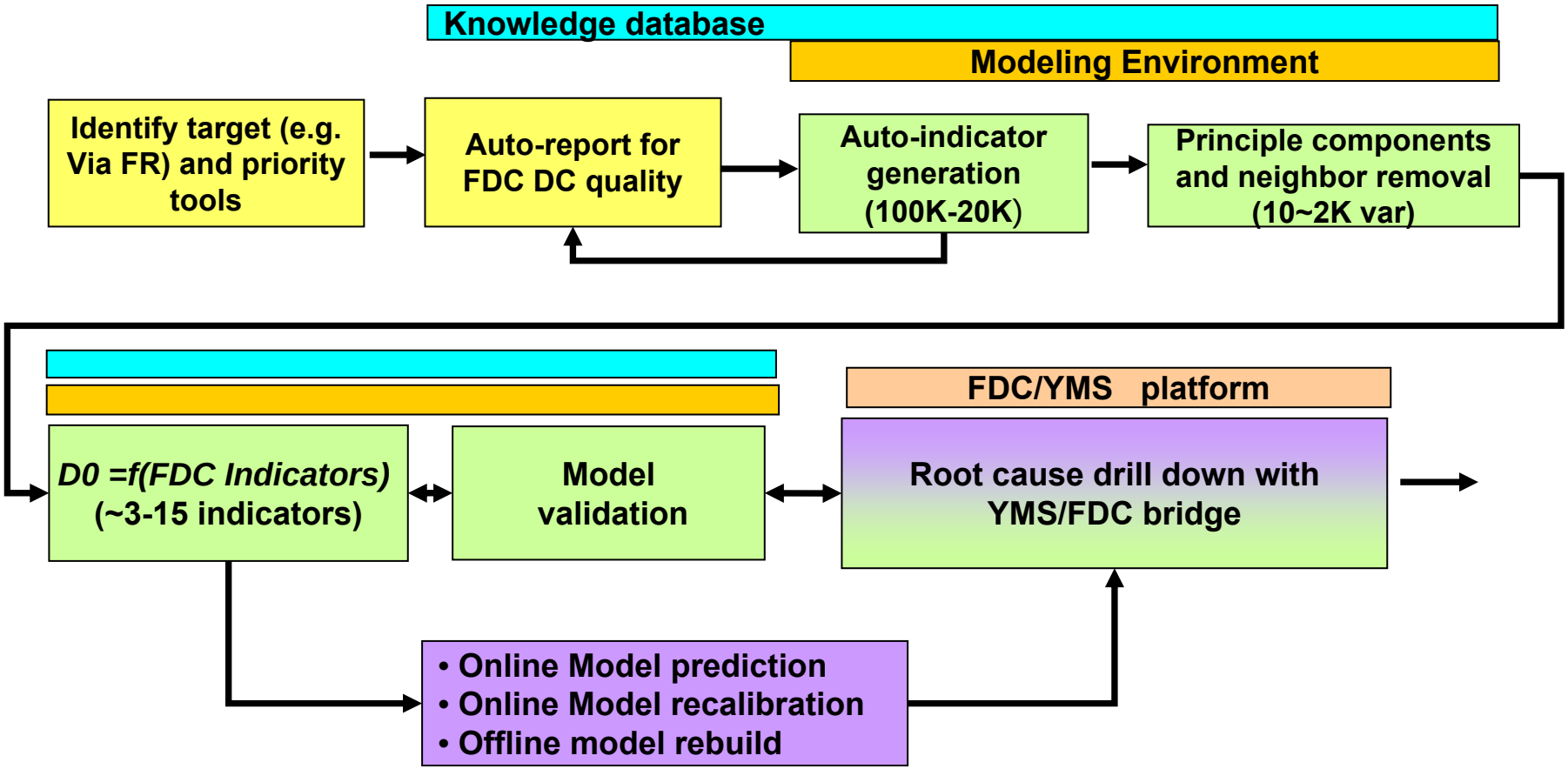
M1-v1 Module Example	
Num of indicators	200,000
Wafers/month	10,000
Num of obs/hr	2.8E+06
Control limit	5 σ
Num of alarms/hr	2

A 5σ control limit generates
~ 2 alarms / hr / module → Unsupportable

Fundamental issues :

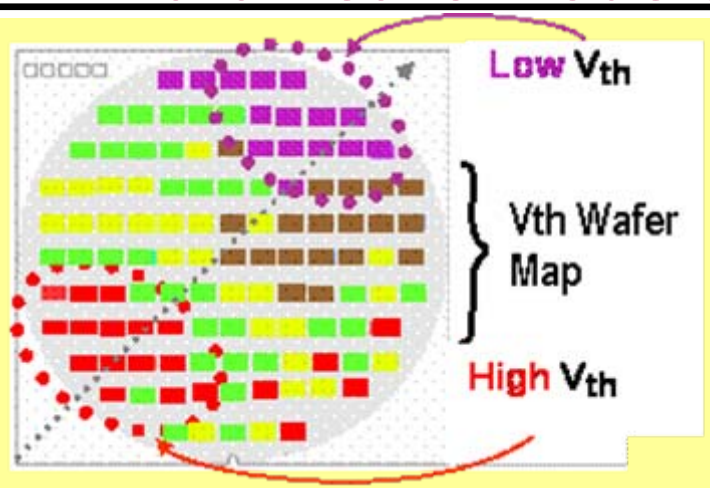
1. Control is not based on yield : hence no systematic way to prioritize FDC monitors (to critical few) based on product & cost impact
2. Poor infrastructure : FDC and YMS in separate databases without alignment from process point of view, and hence not efficiently.

YA-FDC Modeling Work Flow



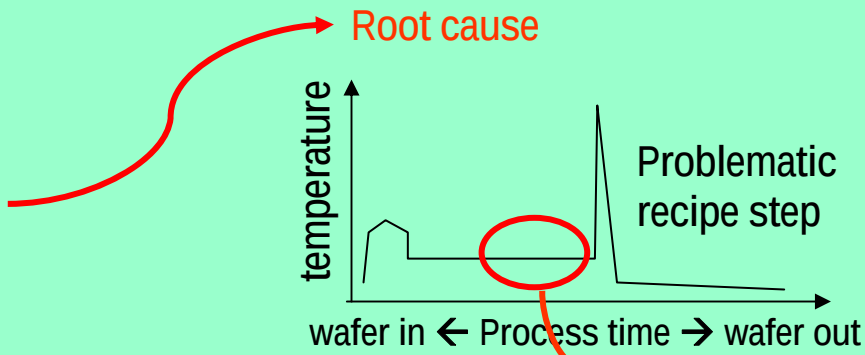
- Model building requires an integration of series of data operations
- Model Output identifies key equipment "indicators" (derived from time-based equipment sensor signals such as temp, pressure, power, flow rate, etc)
- Component parameters are modeled as function of reduced set of key indicators

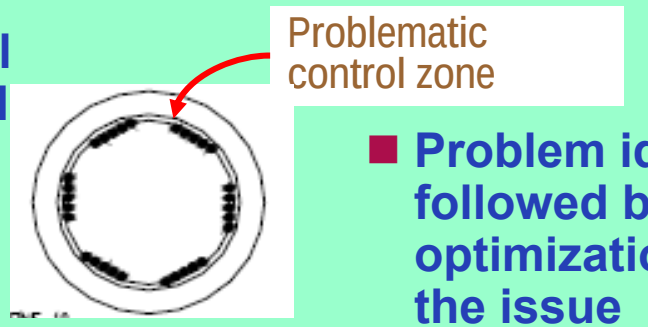
Example 1 : Parametric Models – RTA Impact



- Large within-wafer PMOS V_{th} variation seen by client

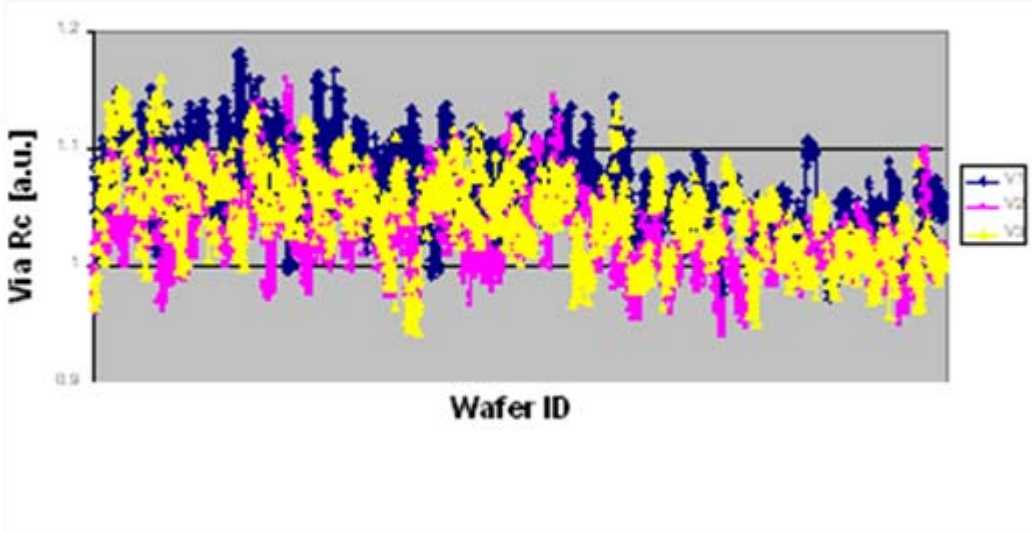
- YA-FDC modeling identified the key yield-critical parameter
- V_{th} variation was caused by stabilization temperature, not spike anneal as expected
- Out of multiple RTA control zones, YA model identified a particular zone as the problem source



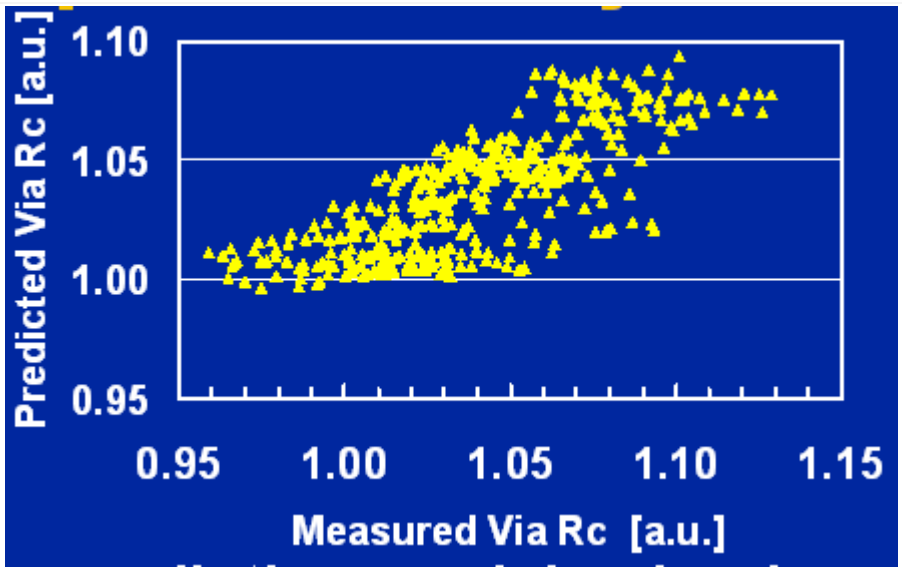


- Problem identification was followed by recipe optimization that eliminated the issue

Example 2 : BEOL Via Rc



Via Rc in Drift 65nm mass production line

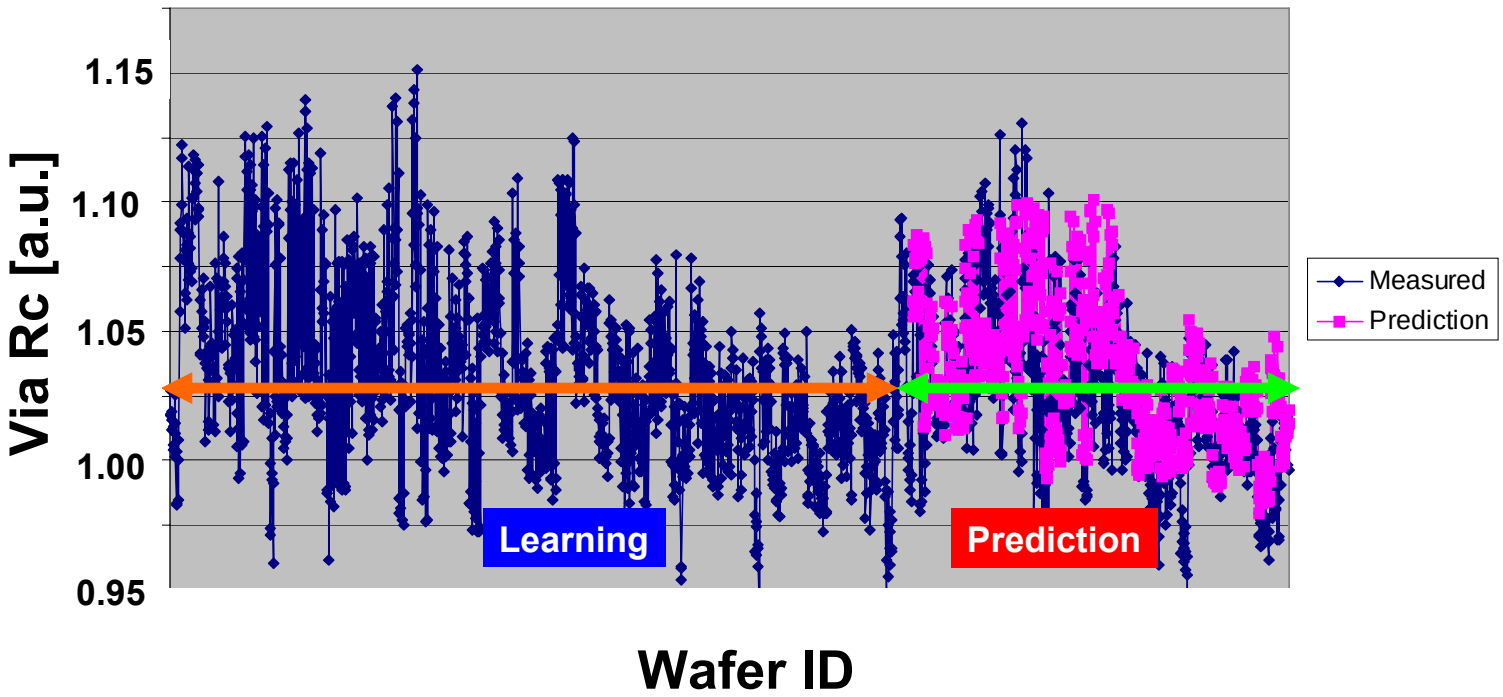


- **Rc prediction model using key indicators shows good predictability**

PVDChamberDcPowerActual-TaN/Ta depositon-stepDuration
PVDChamberDCVoltage-TaN/Ta depositon-mean
PVDChamberDcPowerActual-Ta depositon-stepDuration
PVDChamberDCVoltage-Ta depositon-mean

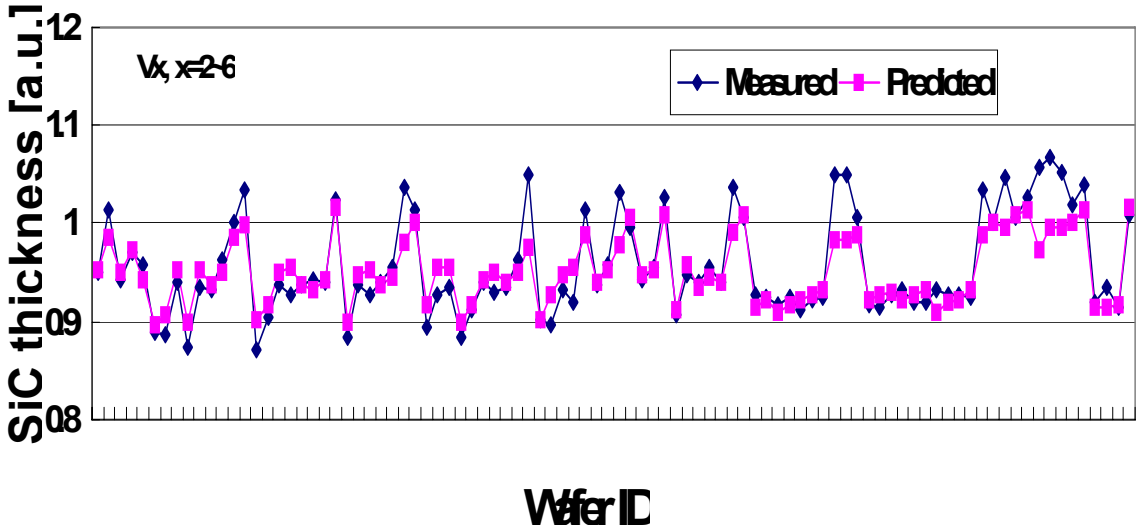
Example 2 : BEOL Via Rc (Cont')

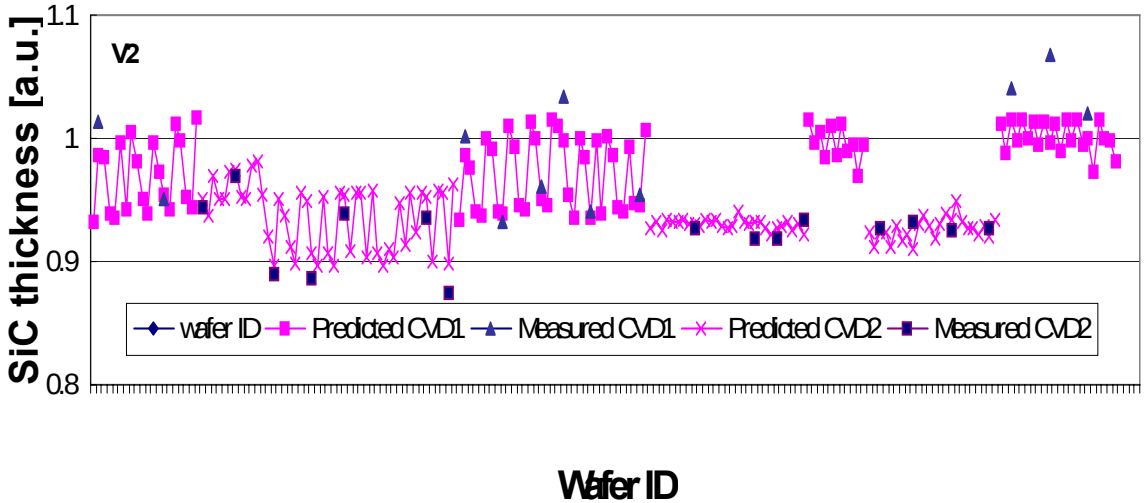
- Online model deployment
- Useful for "tool matching" to reduce variation introduced by multiple tools



- Understanding and control of contact resistances is one key for minimizing device shifts in the field

Example 3 : BEOL ILD Thickness Control





- In this case the YA-FDC model is build to understand the variation of SiC thickness in BEOL (a backend dielectric)
- Since FDC data is available on EVERY wafer, it is able to clearly capture wafer-to-wafer variation (and understand its root cause), which is difficult from normal metrology measurement (which is on 2~3 wafer per lot)
- Can be extended to control BEOL components built from Metal and dielectric layers (caps & indictors)

Summary

→ Take advantage of advanced CMOS nodes without "analog" penalty even when adding components

→ Characterization, Reduction, & Control of Variation is Key

- Deployment of High volume Characterization Infrastructure to facilitate High Precision modeling and PDKs
- Use of advanced "fabric" layout and circuit techniques that are now enabled by advanced node CMOS
- Utilize "Yield Aware FDC" Fabrication Line equipment Modeling Strategies