

Trends in Power Devices

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Trends In Power Devices

Just Talk a little ☺

- In defining new technology, the interconnect between silicon and package must be an equal part of definition, the silicon device is only just a part.
- In recent years not much change in the architect of LDMOS devices
 - Drain engineering such as RESURF and Isolation, etc
 - Lithography scaling for density
 - Improvement in Rsp FOM on the average of about 20% each generation every two to three years but reaching it's limitations
- Today there are many competitive process nodes with similar FOM
- Differentiation is in characterization, robustness, and reliability
 - Improved SOA (safe operating area) robustness
 - Added Channel hot carrier characterization to all MOS devices
 - Innovative drain isolated LDMOS architecture for extreme efficiency and low switching losses
 - Power metal with bonding over active area

Trends In Power Devices

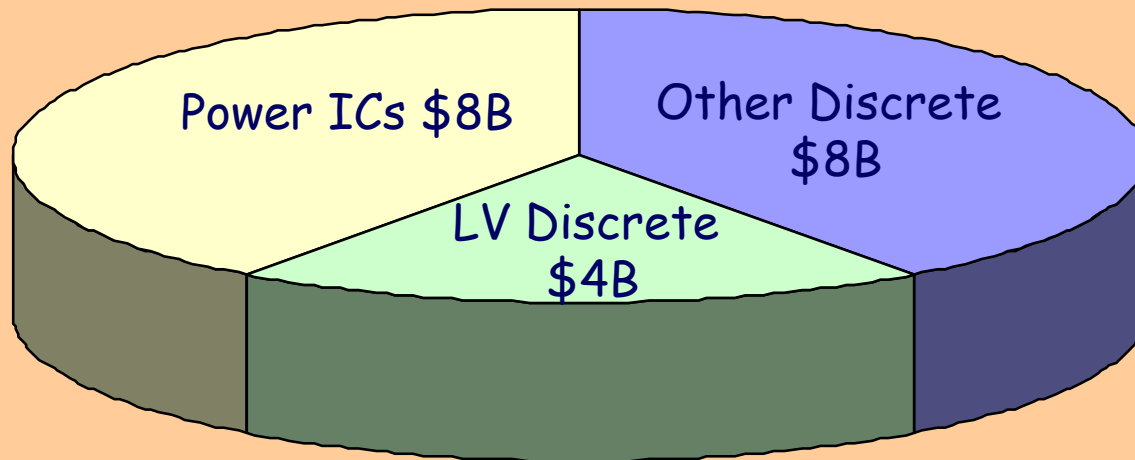
And a little more, Talk ☺

- **Creation of high voltage and low voltage nodes with options**
 - **Allows density and optimization without sacrifice of spacing rules**
 - **Modularity to create simplified flows for innovative and application specific design**
- **Higher speed switching up to 5MHz requires low C hence low Q a newer FOM is RxQ**
- **World class performance QFN, WCSP, and unique power packages**
 - **Many more MCM types becoming common**
 - **Cu wire lower R, higher performance, and lower cost**
- **Discrete power device technology needed for high current**
 - **High current → very low Ron, diminishing returns for monolithic integration Si cost vs discrete solutions.**

Power Device Market

Power Device TAM

Maybe \$20B to \$22B,
12% to 14% growth Yr/Yr



LV = < 40V

Other = > 40V up to 3KV, Si, SiC, GaN

LV Power Device Driver Levels

Battery Levels (V)		Industrial Standard Supply Voltage (V)		CMOS Levels (V)	BCD Tech Levels V (Abs Max)
0.8 – 1.2	NiMH	3.3	Ind Comp supply	1.2	1.8
1.5	Alk	3.6	1 White LED	1.5	3.3 (3.7)
3.0	2 Alk/NiMH	5.0	Ind Comp supply	1.8	5.0 (6.7)
4.3	LiIon	10.0	Industrial supply	2.5	20
6.3	3 PbSO4	12.0	Ins Comp supply	3.3	30
8.6	2 LiIon	15.0	Industrial Supply	5.0	40
9.0	6 Alk	24.0	Industrial Supply	10.0	55
12.6	6 PbSO4	36.0	String 10 WLED	15.0	65
12.9	3 LiIon	40.0	Auto Load Dump	20.0	85
17.2	4 LiIon	48.0	Telecom / Safety	24.0	110
25.2	2 car batt	60.0	Automotive Regulated Power Supply		
Mobile					

HV Power Device Driver Levels

Battery Levels (V)		Tech Levels V (Abs Max)
110	Tele / Solar	120
200-300	Med / Solar	250 - 400
240	On/Off line AC	800
240	Ind Motor/ Traction	900
KV	Trains / Boats / Solid State Power Conversion	1.2 -3.0KV

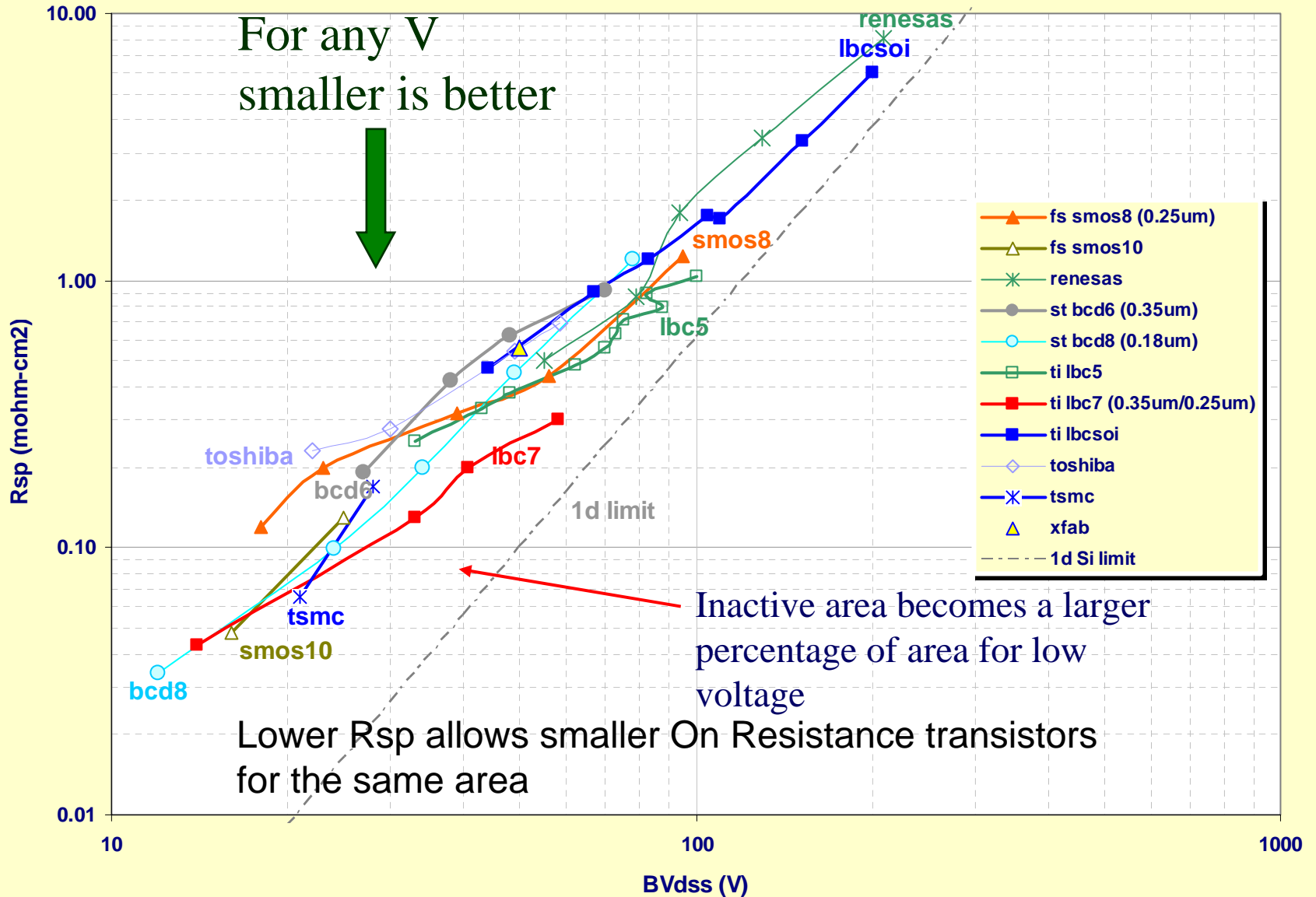
Some of these can be integrated for driving and low current, otherwise most likely they would be a discrete solution and may be material other than Silicon, eg GaN or SiC

Resistance and Voltage

- The old and most talked about figure of merit is “Specific on resistance” R_{sp} vs BV_{dss}
- And of course its important sense it relates to power device size and competitiveness
- Silicon area vs process complexity, cost money

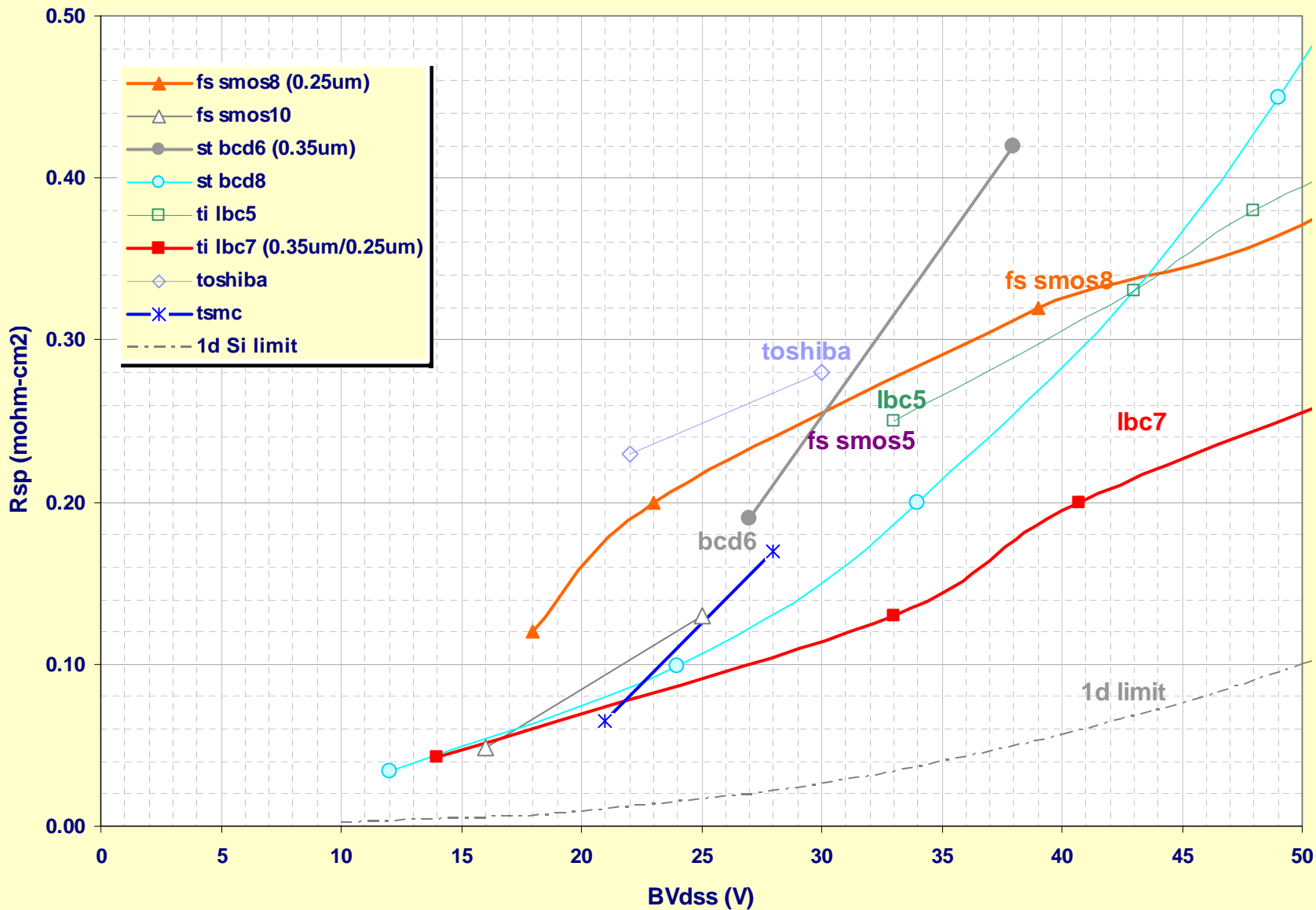
Integrated LDMOS Performance

Ldmos benchmark (10 to 200V)

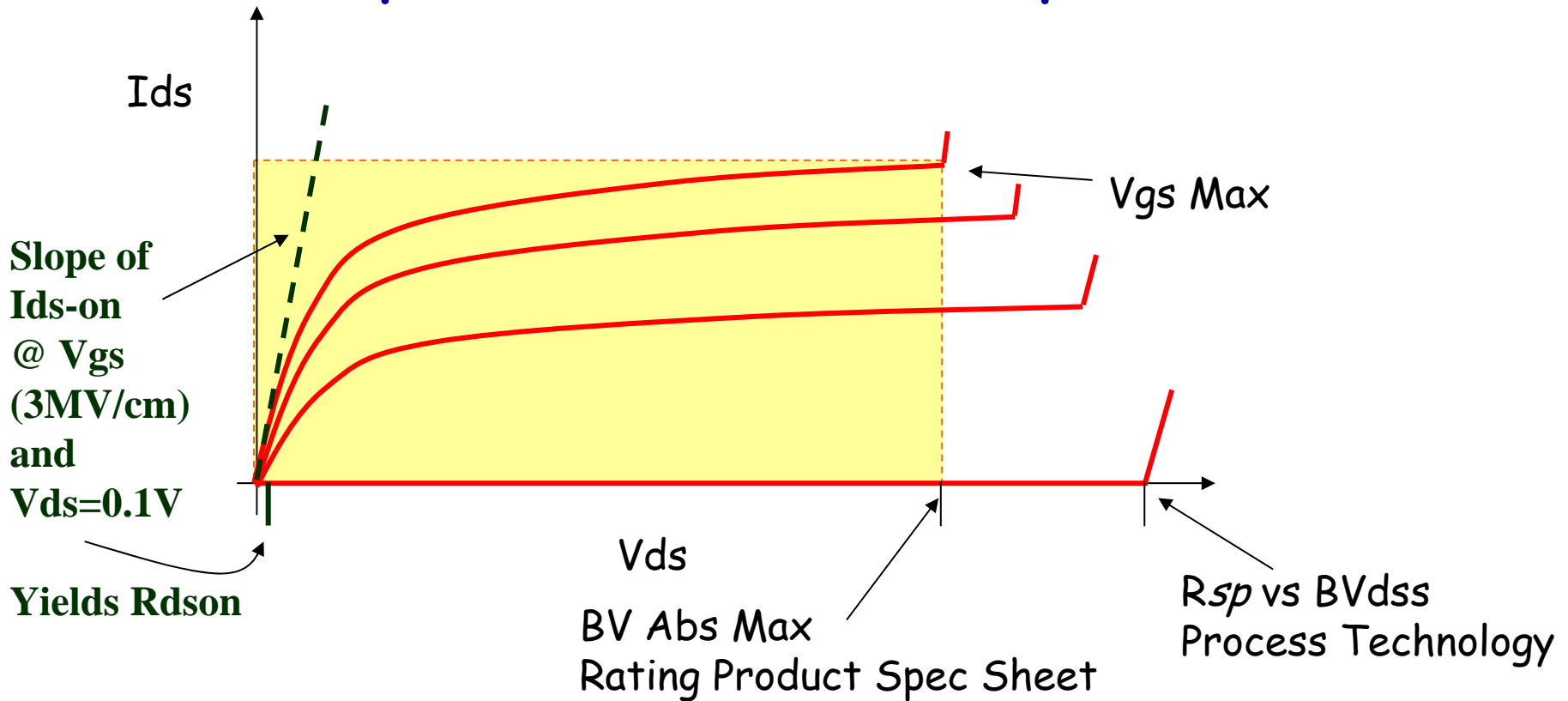


Zoom on LV LDMOS

Ldmos benchmark (low voltage)



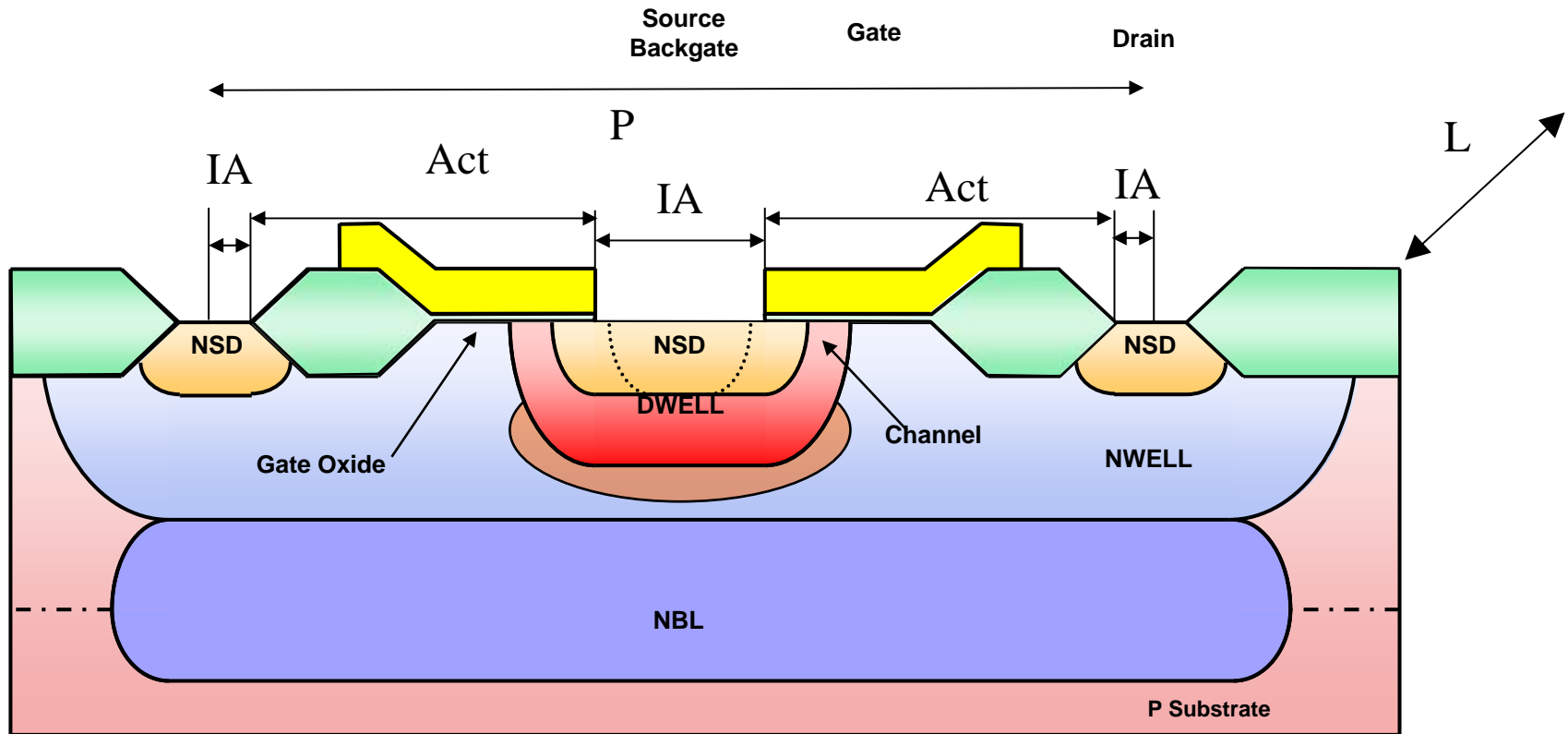
FOM Specific On Resistance R_{sp} vs BV_{dss}



Law of BV vs R_{sp} - The closer you can get BV_{dss} to rated BV, the lower realized R_{sp}

$$R_{sp} = R_{ds-on} \times Area$$

Some LDMOS Devices for Integrated Power ICs



- L = length of stripe
- P = Pitch
- Act = Active Area
- IA = Inactive Area

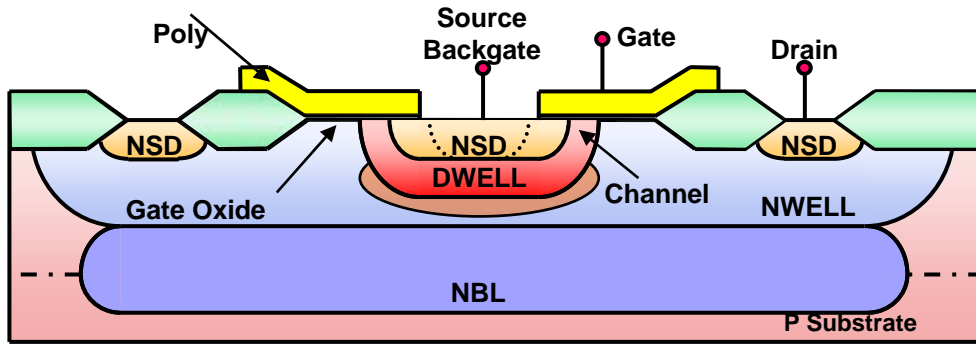
- Lithography scaling affects Inactive Area
- Active area is a function of R_{ds-on} determined by:
 - Silicon device physics, metal, and gate drive

$$R_{sp} = R_{ds-on} \times Area$$

$$Area = P \times L$$

$$Area = (IA + Act) \times L$$

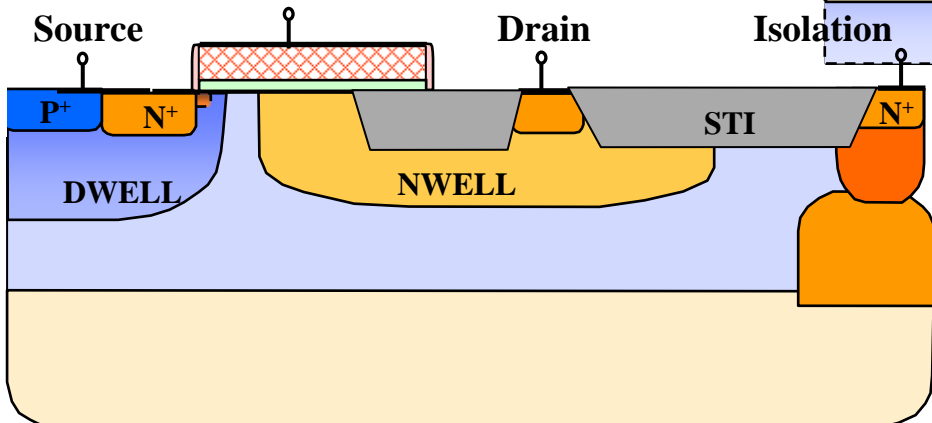
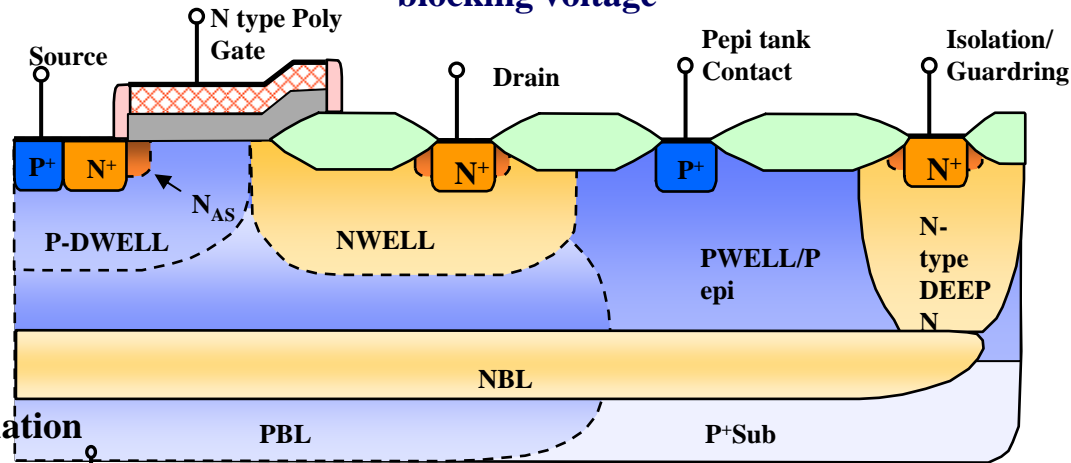
Some LDMOS Devices for Integrated Power ICs



- LDMOS = Lateral Double-Diffused MOS
- Channel Length Set by Out-Diffusions
- Asymmetric N-Channel MOSFET
- FoM = Specific ON-Resistance (R_{sp}) (Normalized area)
- Very low off state leakage for high blocking voltage

•LBC5 LDMOS, MEV Dwell, shown symmetric about source region, SOA high current / voltage

•LBC7 Modern LDMOS, Drain isolated technology, density and efficiency, mobile solutions



•LV or HV LDMOS using Shallow Trench Isolation "STI", very dense SoC Solutions, DI technology

Robustness and Reliability

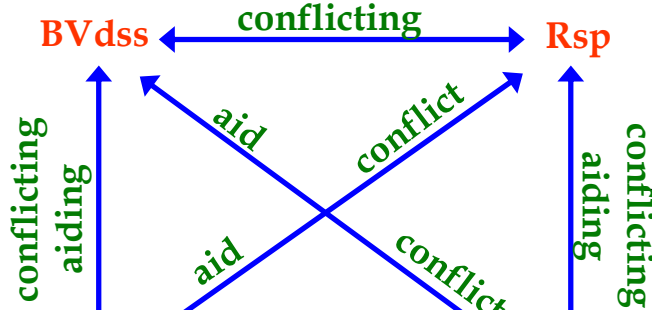
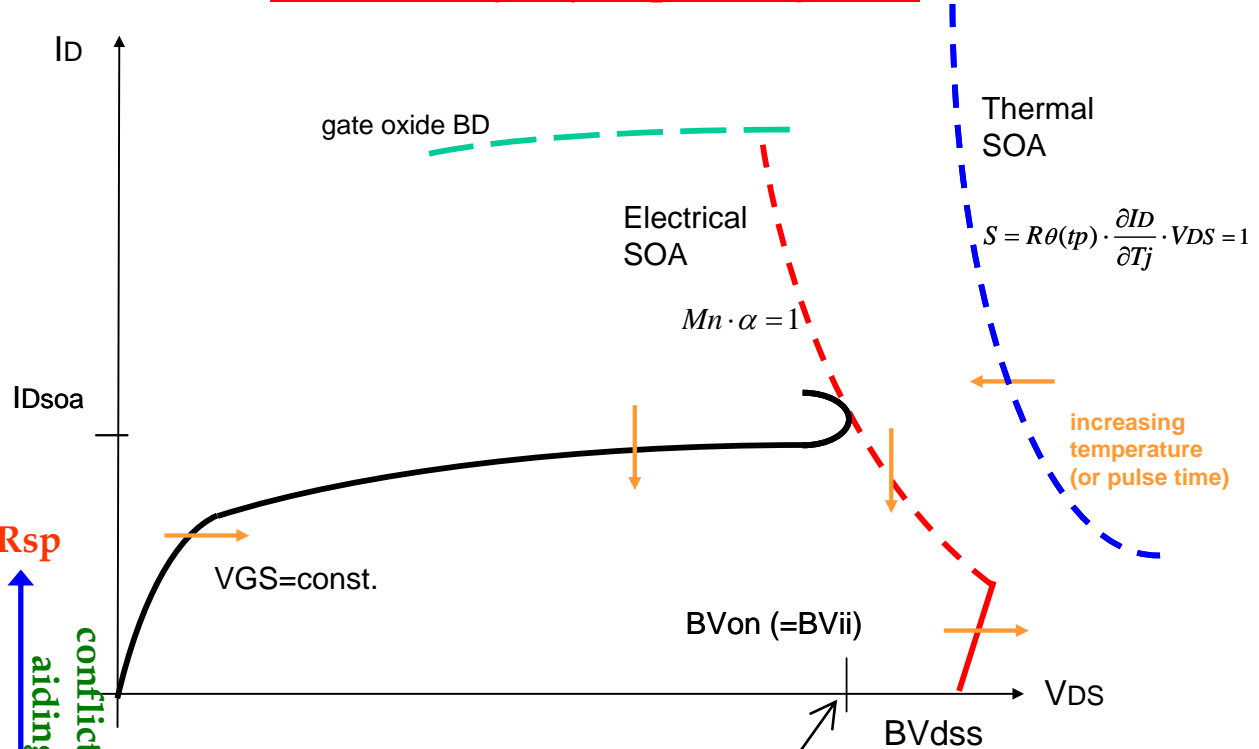
- **Good on Resistance is no good if the power device does not meet the rated voltage**
- **And it has to be able to be used reliably in any application for the rated voltage**

Safe Operating Boundary Characterization

Hot Carriers can:

- Degrade V_t
- Degrade I_{dlin}
- Degrade I_{dsat}
- Degrade g_m
- Devices for Analog insure 10 year lifetime <10% drift DC bias

Two kinds of Safe Operating Area

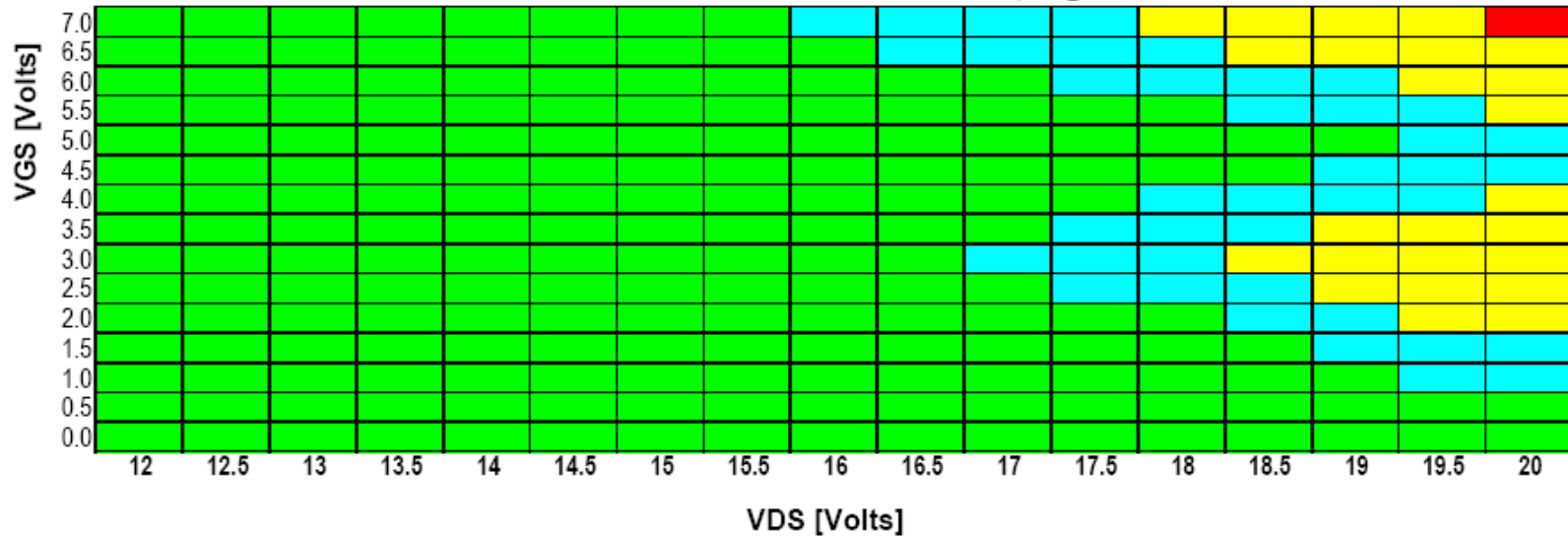


Usable Range

- Power devices designed to meet BV spec based on electrical SOA.
- Electrical or thermal may determine the boundary of usability.

CHC SOA Design in Reliability

CHC Duty Cycle Operating Area
 Based on 10% Shift in I_d -Lin (worst case parameter)
 LBC7 20V HSD LDMOS #104; $L_g=1.2\mu m$



Duty Cycle = 100%
 $TT_{10\%} > 10 \text{ yrs}$



10% < Duty Cycle < 100%
 $1 \text{ yr} < TT_{10\%} < 10 \text{ yrs}$



1% < Duty Cycle < 10%
 $0.1 \text{ yr} < TT_{10\%} < 1 \text{ yr}$



0.1% < Duty Cycle < 1%
 $0.01 \text{ yr} < TT_{10\%} < 0.1 \text{ yr}$



Duty Cycle < 0.1%
 $TT_{10\%} < 0.01 \text{ yr}$

- Channel Hot Carriers Especially important with the trend toward thinner oxides

Off State Performance

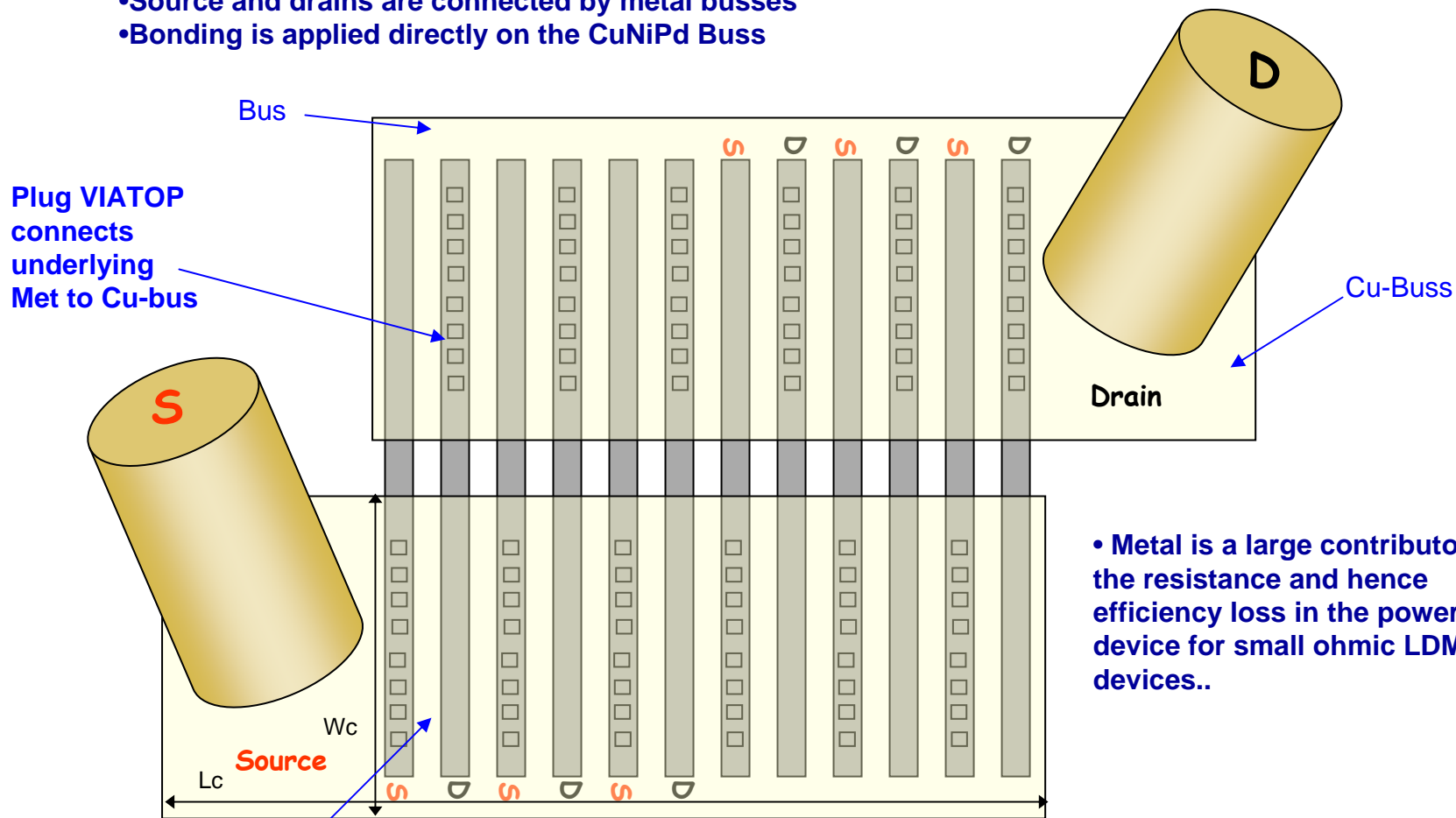
- Ideally zero leakage would be nice 😊
- Off state losses is very important in today's energy efficient green world
- It simply means using less electricity
- In Mobile applications it also means longer battery life between charges
- **With the trend in thinner oxides, lower voltage drive levels, and smaller pitches, reverse leakage could be a limiting factor!!**

Power Metal

- **Metal resistance in lateral devices creates a resistive drop because of the lateral current flow in the metal**
- **This is a resistive loss but also affects the transistor operation in terms of “de-biasing”**

Method of constructing an LDMOS

- LDMOS is made up of long striped geometries of the silicon device
- Source and drains are connected by metal busses
- Bonding is applied directly on the CuNiPd Bus

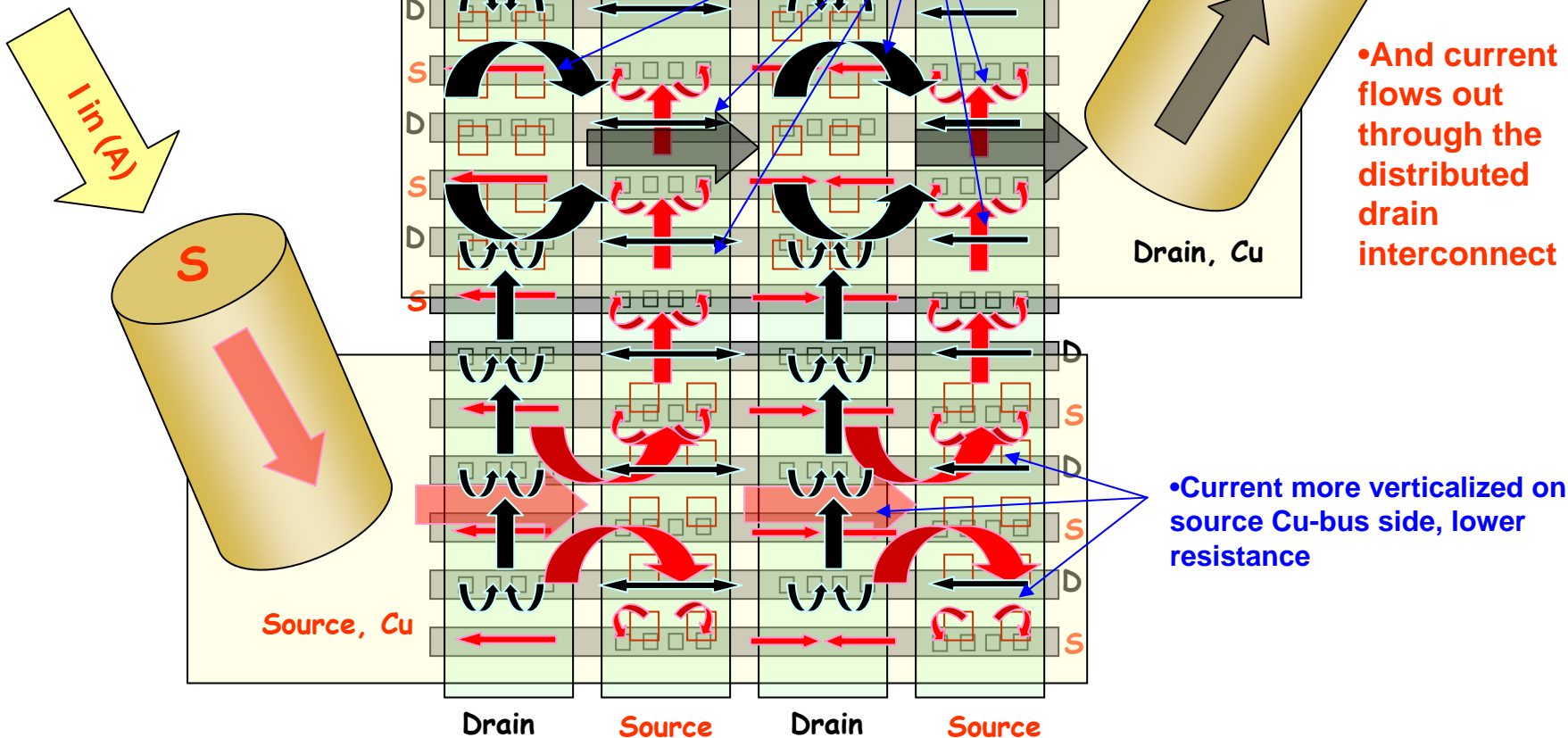


- Metal is a large contributor to the resistance and hence efficiency loss in the power device for small ohmic LDMOS devices..

**** So decreasing R_{sp} of the LDMOS results in diminishing returns if the layout is limited by metal interconnect EM rules. Basically silicon area would be wasted.**

- Current flowing laterally in the metal creates resistive voltage drop
- On the source side the voltage drop is above ground so
 - $V_g - V_s = V_{gs}$ effectively reduces gate drive
- On the drain side the drop is below supply so
 - $V_d - V_s = V_{ds}$ effectively reduces and negatively offsets V_{ds}

- Lateral current in source metal, higher resistance

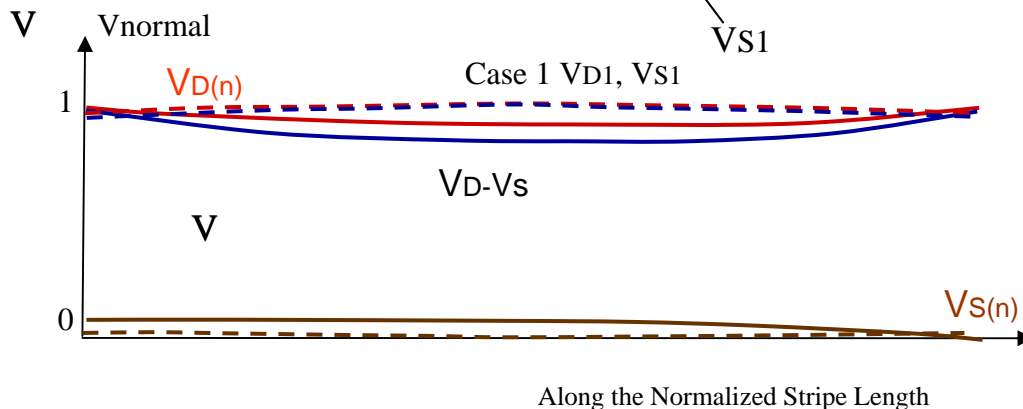
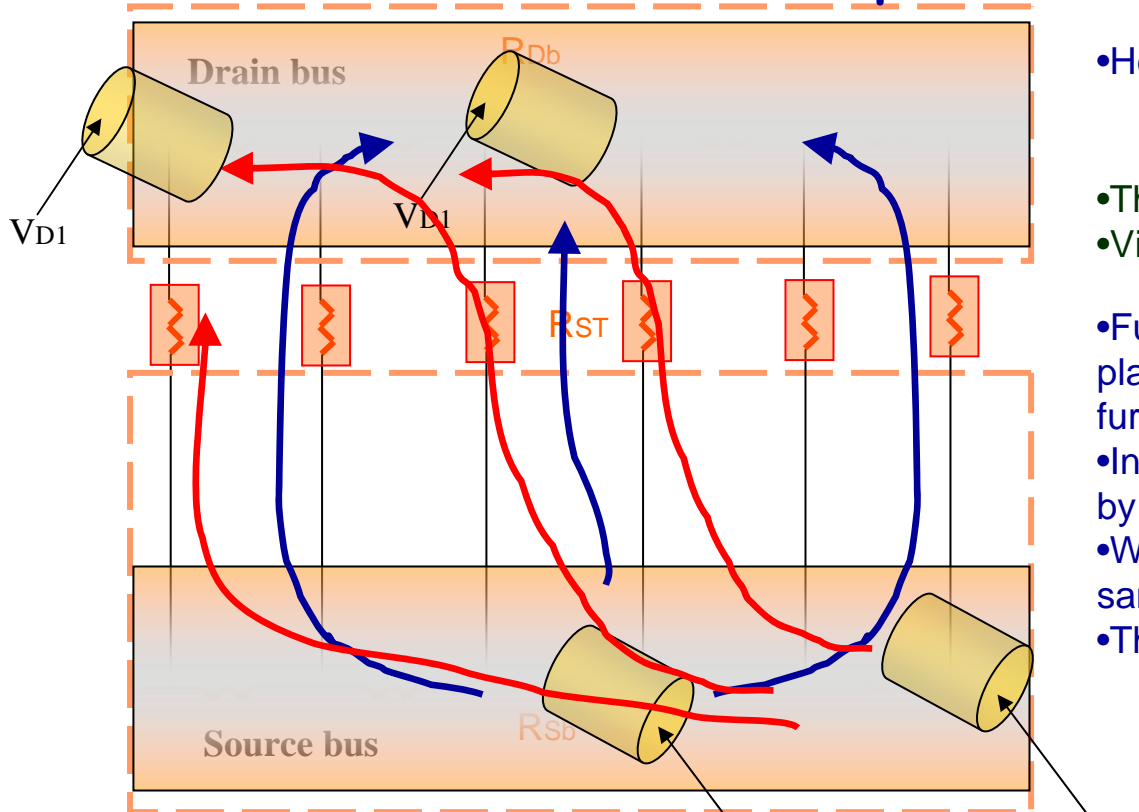


- Current flows in through the distributed source interconnect

So the use of geometry and low resistance metal is key to

- Verticalizing current flow
- Silicon resistance efficiency
- Uniform switching behavior

Thick metal Impact!



•Here is how it works

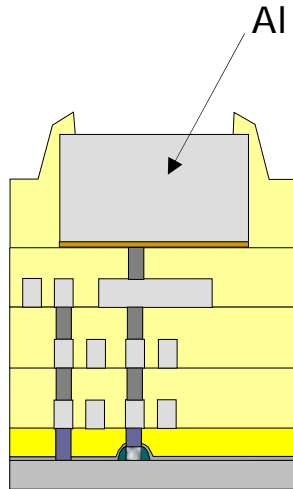
- Thick plated CuNiPd
- Virtually eliminates bus resistance
- Further the CuNiPd allows internal bond placement, for large designs critical for further reduction of bus resistance.
- In the example bus resistance is reduced by four, it is like two halves in parallel
- When there are two bonds spaced on the same bus it is like one eighth!
- The new curves are shown as dotted lines.

•Note, if trying to build a transistor of $20\text{m}\Omega$, a couple of squares of CuNiPd could be $2\text{m}\Omega$, or 10% of the resistance, it means that the silicon part will need to grow by 10%. !!

• Just imagine building a 10 or 5 $\text{m}\Omega$ switch!!

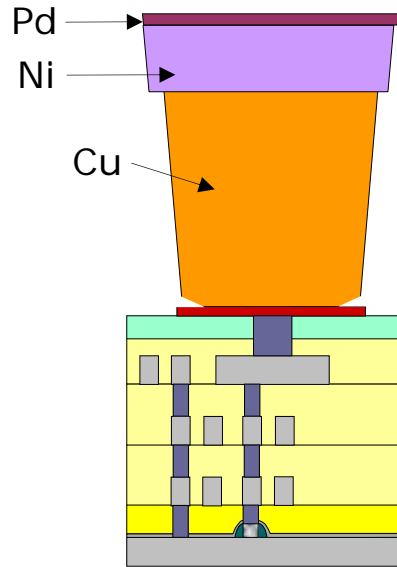
Power Metal Possibilities

M1-M3



Thick AL

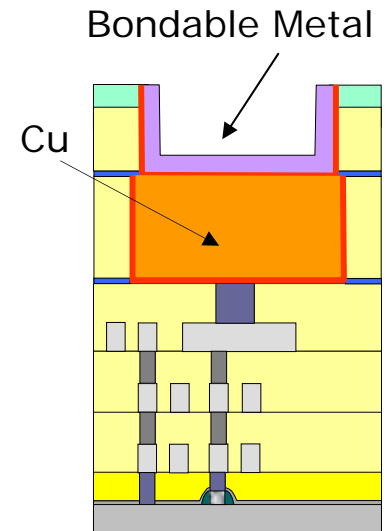
- (2um to 4um?)
- Higher P_s
- Limited bond over active
- Lower cost
- Manufacturability any where
- Good enough
- FET Ron > 120 m Ω



Thick Plated CuNiPd

- (6um to 15um?)
- Low P_s
- Bond over active
- Special process
- Limited manufacturing
- Good for low Ron products
- FET Ron < 50 m Ω

- (2um to 3um?)
- Medium P_s
- Bond over active
- Special process
- Limited manufacturing
- Low stress
- Good isolation
- FET Ron 40 to 120 m Ω



Thick Cu Damascene

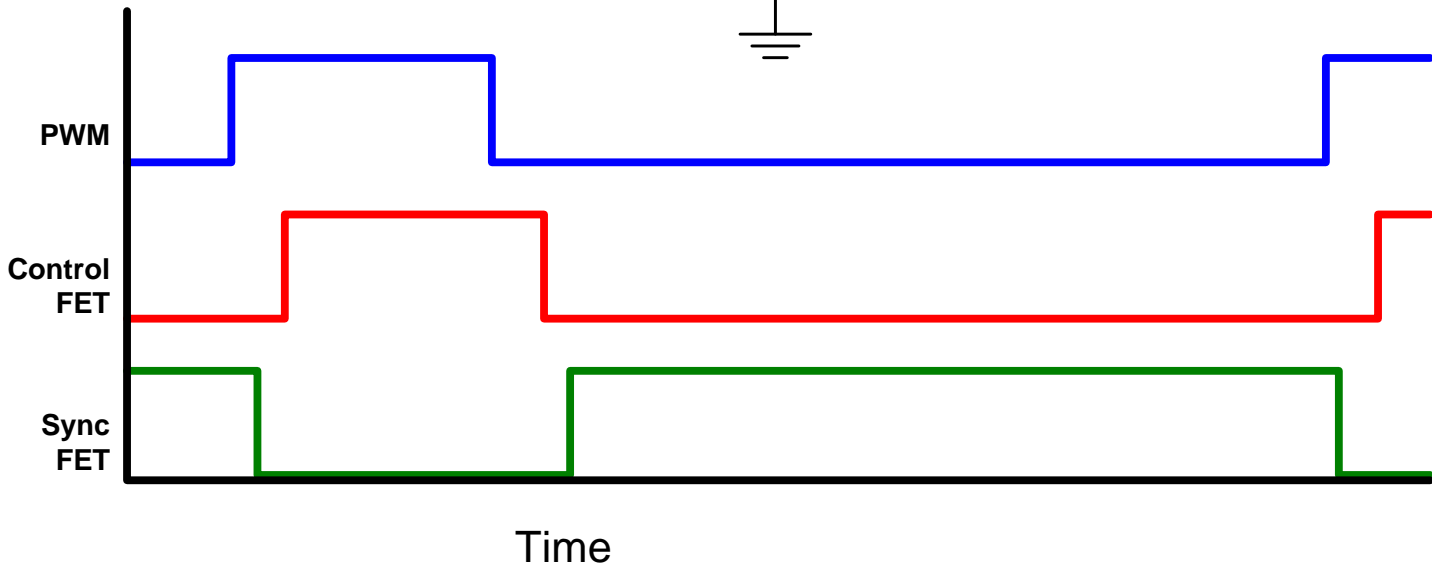
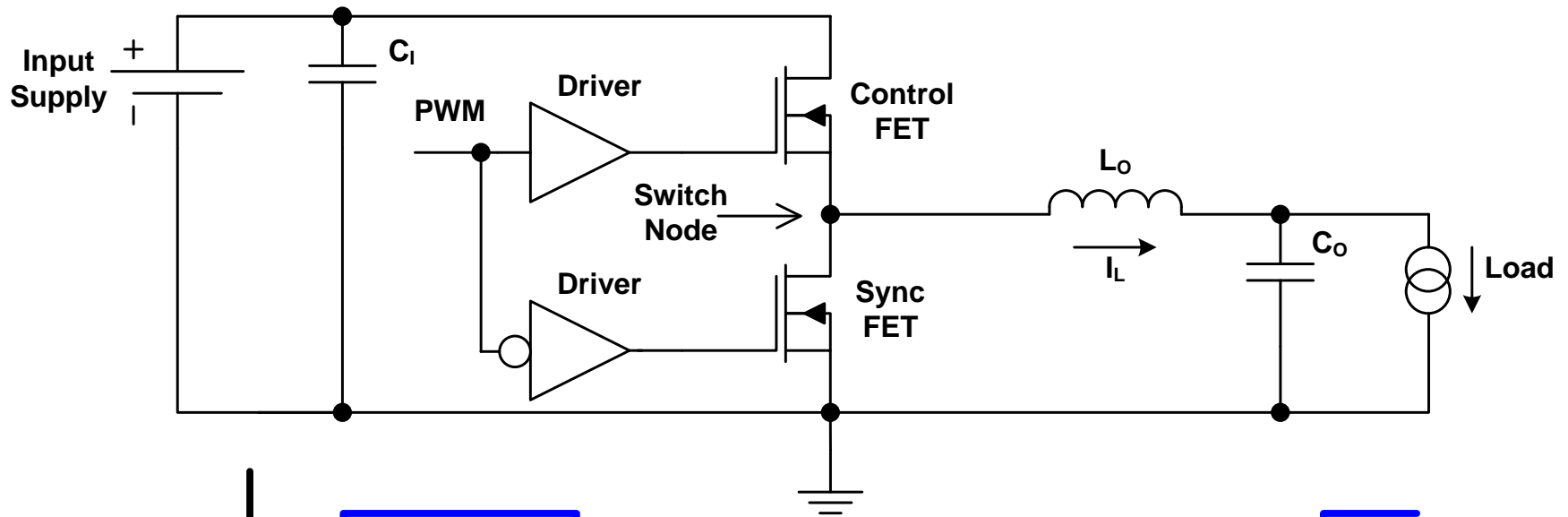
Summary of Operating States

- Rsp vs BV is still an important FOM target
- The power device has to be robust and reliable in all operating states
- Low voltage reverse leakage is extremely important
- Smaller line widths limit the stripe length because of metal resistance and EM properties
 - This may mean more metal layers are required , at added cost ☹️
 - Or Innovative geometry and layout methods
- Metal effects can defeat the effort in reducing Rsp
- This is especially an issue with Low Voltage devices having a very small pitch

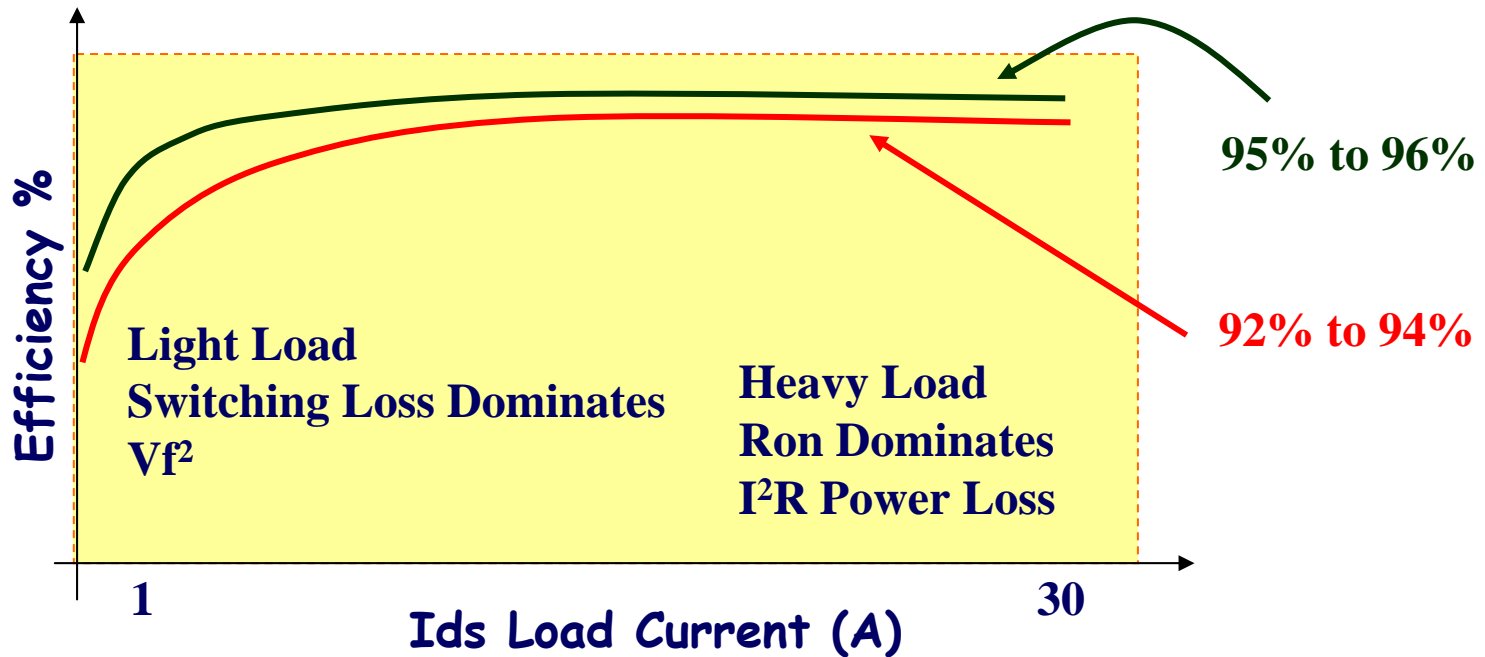
Efficiency and Switching Losses

- **The trend in power conversion is to switch at higher frequencies**
- **(200kHz-600KHz) →→→(800KHz-5MHz)**
- **Allows for smaller external inductors and capacitors, so lower cost and energy savings**
- **But creates trouble for the device**
- **$R \cdot Q$ becomes important FOM**

Synchronous Buck DCDC Conversion 101

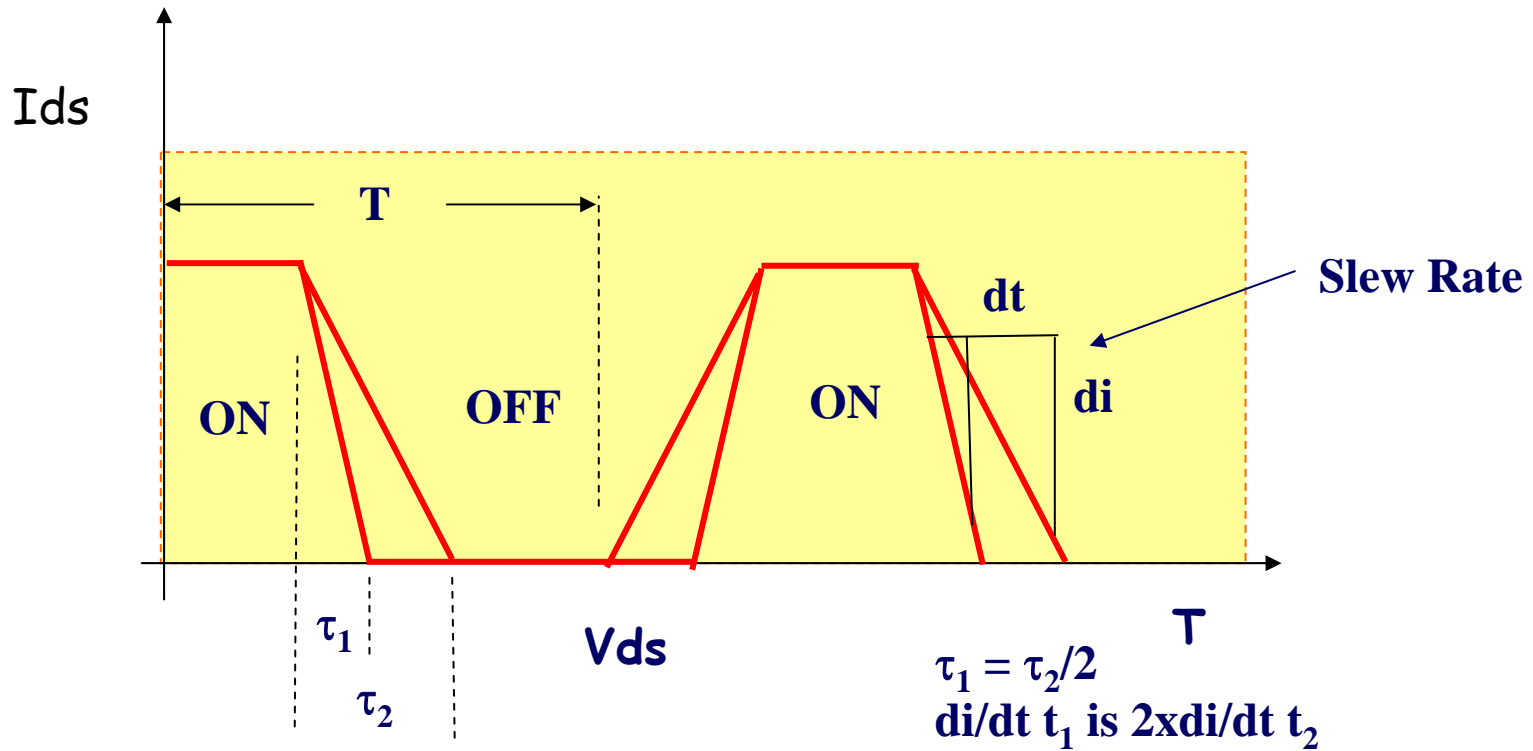


Efficiency and Switching



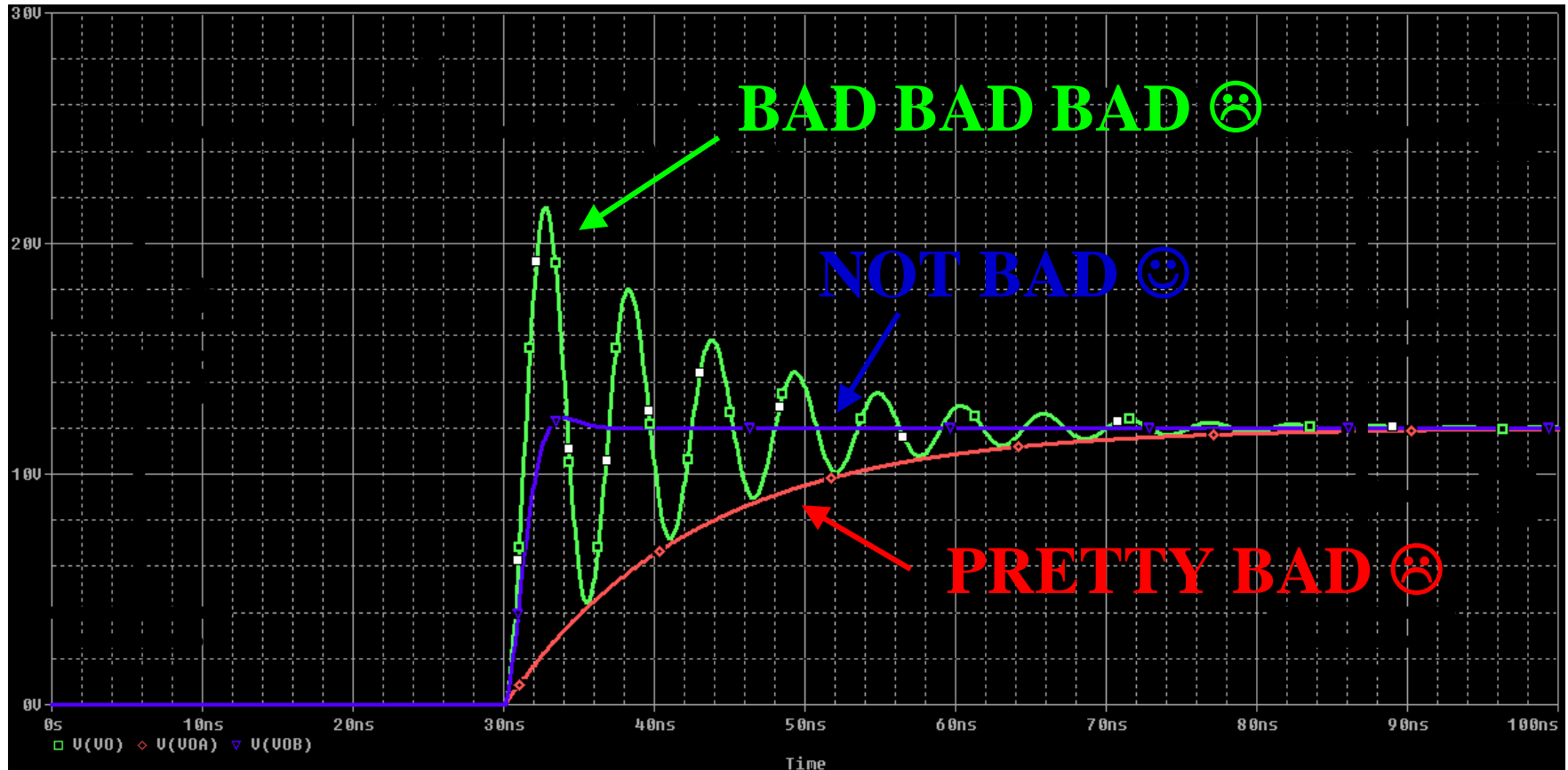
- Efficiency is all about power in vs power out,
- Any loss of power is an efficiency loss
- In today's environment this energy savings is extremely important
- At low current energy loss is dominated by switching capacitance losses
- At high current energy loss is dominated by Resistive losses
- Higher switching speed can provide higher overall efficiency 😊
- And a big improvement in light load efficiency 😊

ON and OFF



- For on / off cycle T to get smaller, or $f=1/T$ the switching frequency /rate gets higher / faster, then:
 - τ turn-on and turn-off transition time has to get faster also
 - But! this means a much higher di/dt ☹
 - And this causes many problems ☹

LC Ringing on the Switch Pin 101 During Fast Switching



- High ringing is perceived as bad and could result in damage
- Too much damping is not good also
- What is best is to have some overshoot and fast settling
- But this is not an easy task for fast switching with all of the C's and L's at play

Diode Reverse Recovery Switch Loss 101

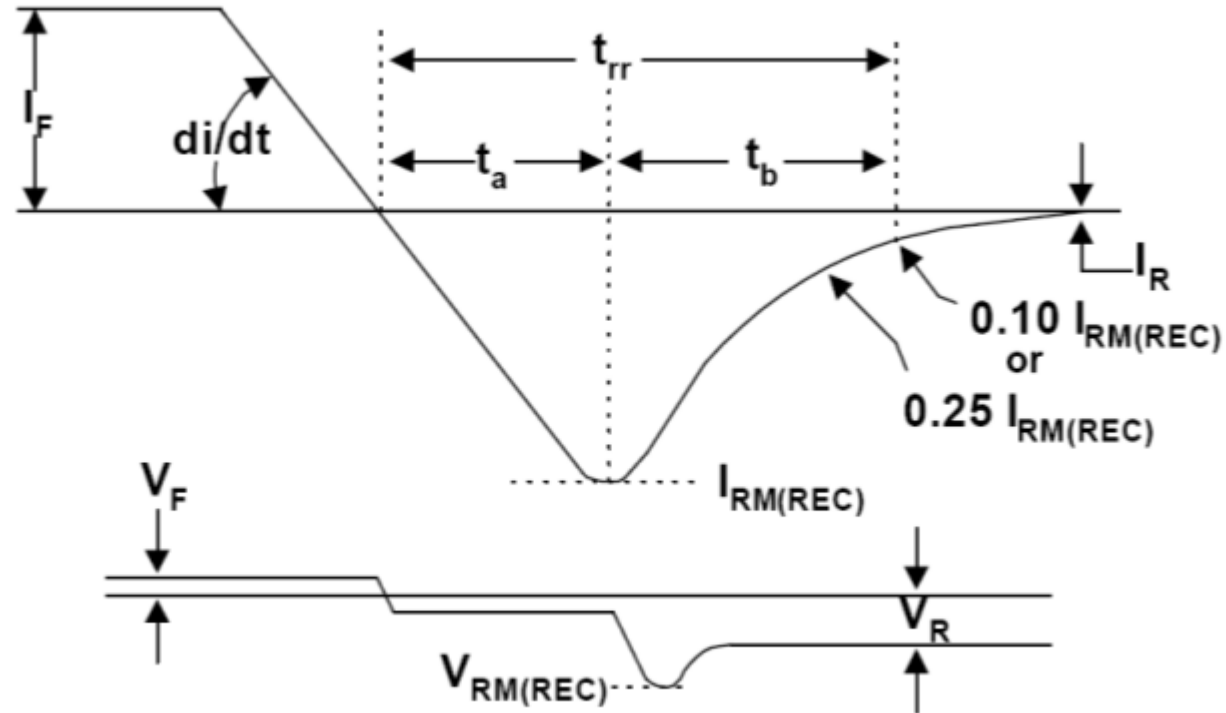


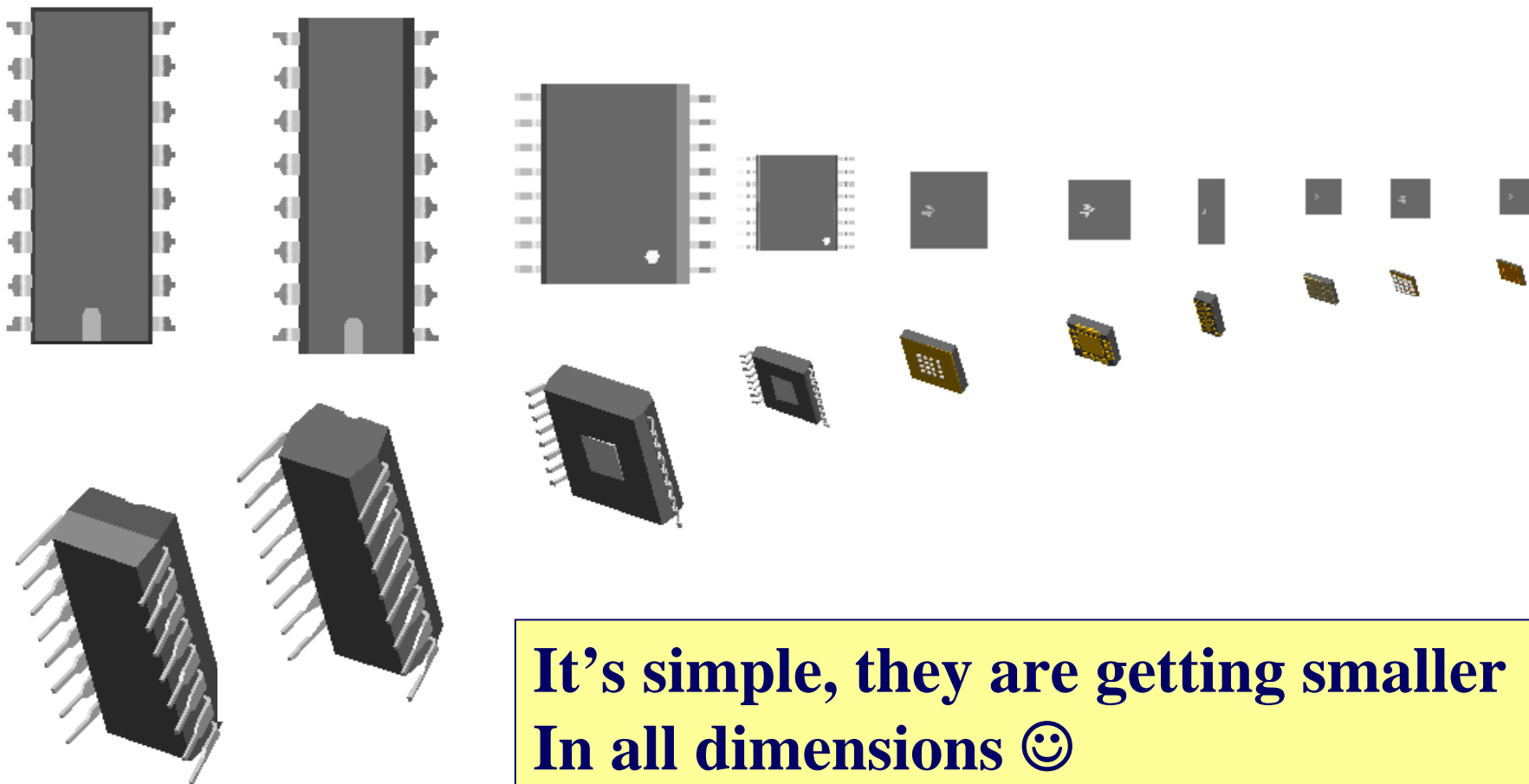
Figure 1. Typical Rectifier Response for Reverse Recovery

- Lower switching capacitance will reduce the amount of stored charge and hence lower reverse recovery losses for faster switching
- Smart device integration can also minimize stored charge

Summary on Switching

- **Higher switching frequency is a desired design and application need**
 - It allows for smaller system components that use energy and are expensive with large form factors
- **Speeds are approaching 2 – 3MHz heading for 5MHz**
- **Lower device capacitance, including Miller capacitance along with reduced reverse recovery is necessary**
- **This is a challenge to device design**

What's Happening With Packages

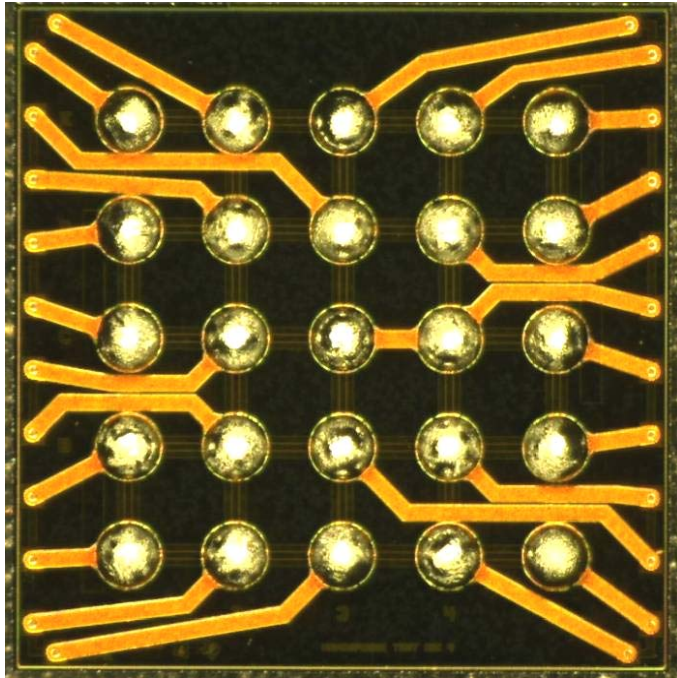


**It's simple, they are getting smaller
In all dimensions ☺**

WCSP Miniaturization Trend

25pin example

0.5 mm Pitch



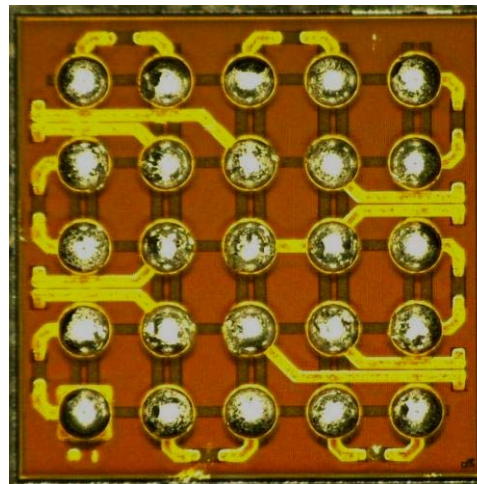
9.61 mm²

(3.1x3.1)

(100%)

Mass Production

0.4 mm Pitch



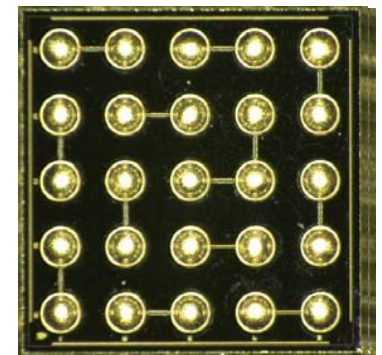
4.84 mm²

(2.2x2.2)

(50.4%)

Mass Production

0.3 mm Pitch



2.56 mm²

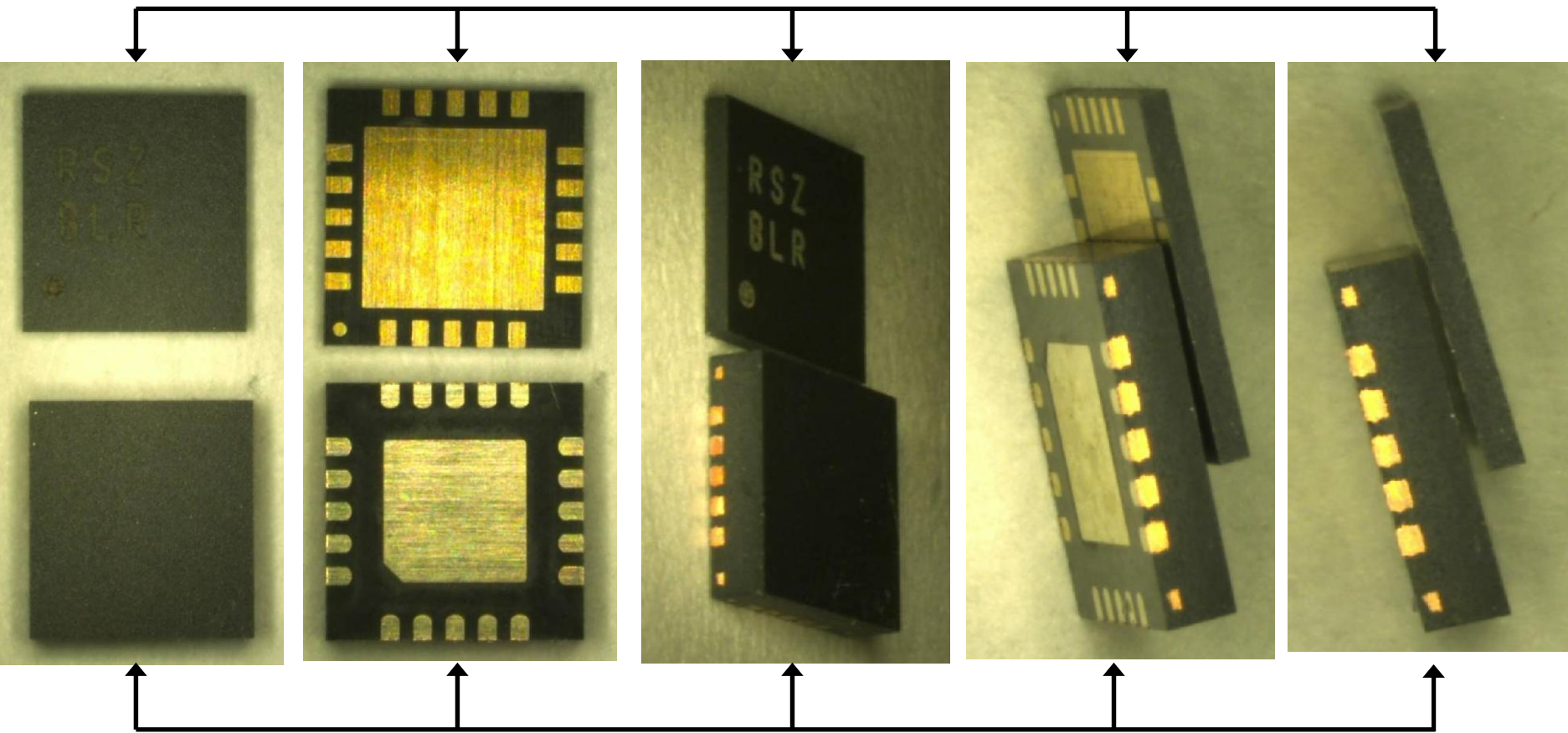
(1.6x1.6)

(26.6%)

Samples Available

QFN Package

0.40 mm Thin QFN Package



Standard 1.0 mm thick QFN

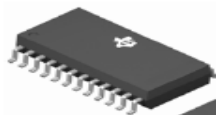
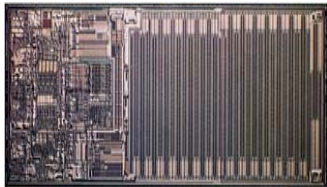
Monolithic Integration of Power

20V Vin DC/DC Synchronous Switch-mode Integrated FETs

0.8-0.6um

6A Buck

- Ron = 59 mOhms
- Efficiency at 1.8V = 83%
- IQ shutdown = 1mA
- FSW 280 to 700 KHz
- Die Size 7.91 mm²

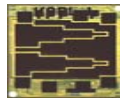


TSSOP20

0.35-0.25um

6A Buck

- Ron = 45 mOhms
- Efficiency at 1.8V = 88%
- IQ shutdown = 1uA
- FSW 200 KHz to 2 MHz
- Die Size 1.39 mm², 5.7x reduction



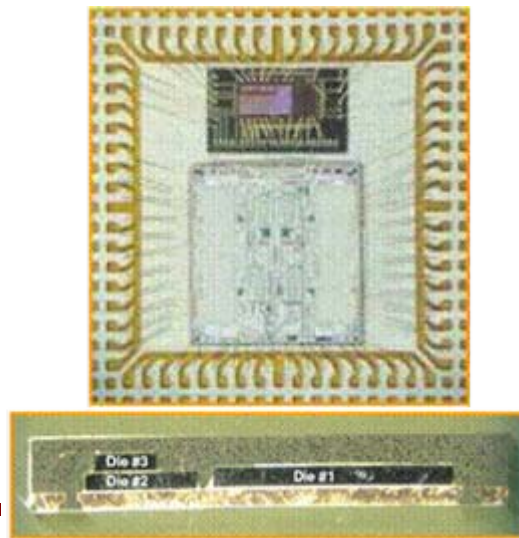
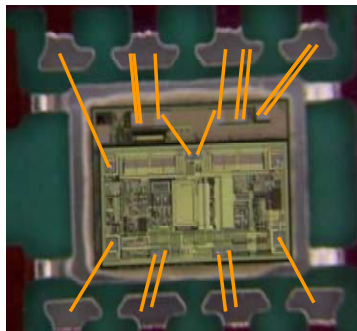
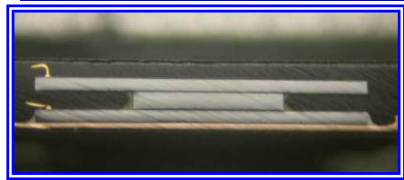
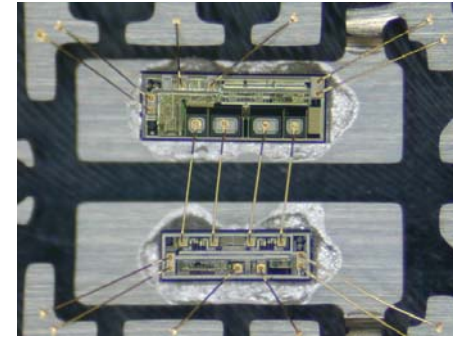
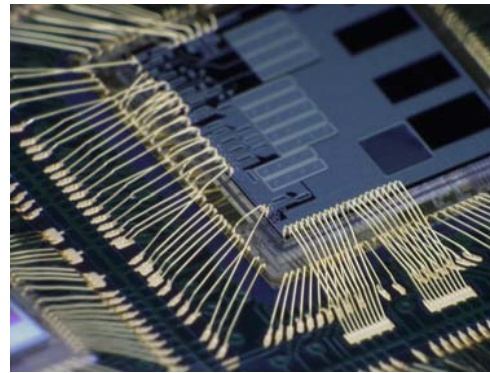
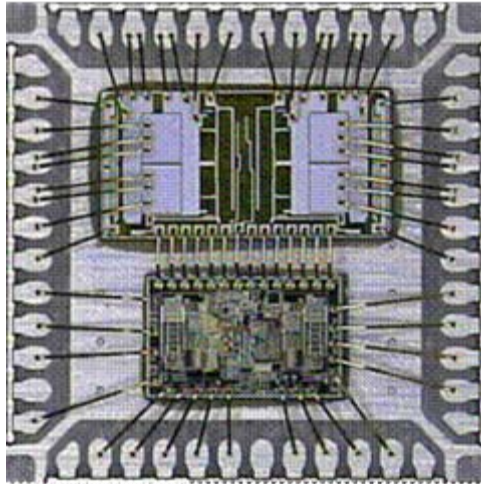
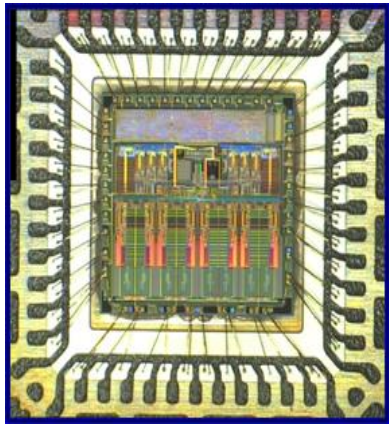
3x3 QFN 16
8X reduction

0.18 – 0.13um

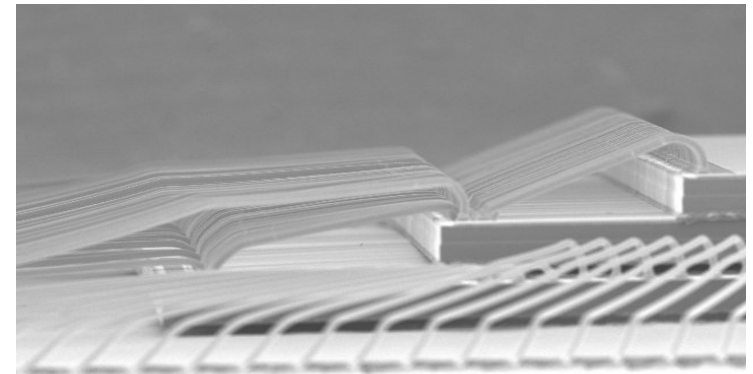
- I don't know ?
- Rsp not much better
- Power density is high
- But if you need a digital block
 - Integrated with >60K gates
 - OK
- IQ may be higher depending on Chore CMOS usage

- For 20V LV device scaling allows significantly reduced die and package size and increased on state and off state efficiency.
- Quiescent current is reduced by 1000X.
- Die size and package size very important care about, provides an opportunity for customer

Multi-Chip Packages

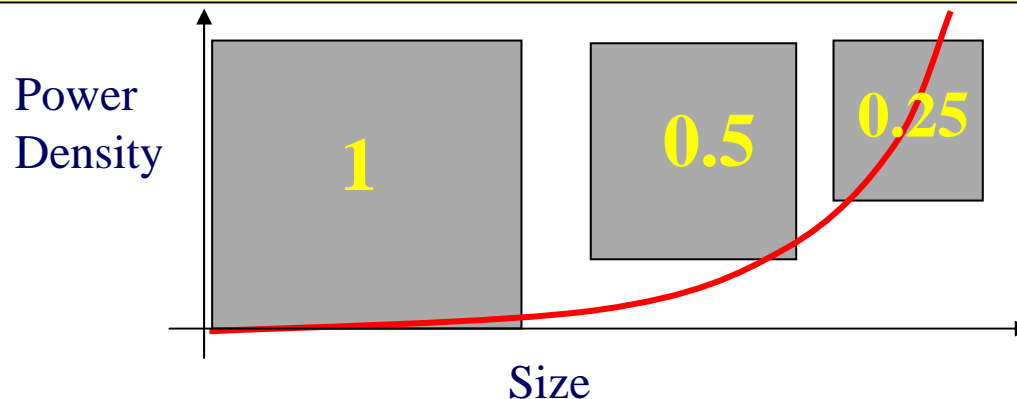


- ✓ Reducing IC & PCB complexity
- ✓ Improving performance
- ✓ Enabling combined functions



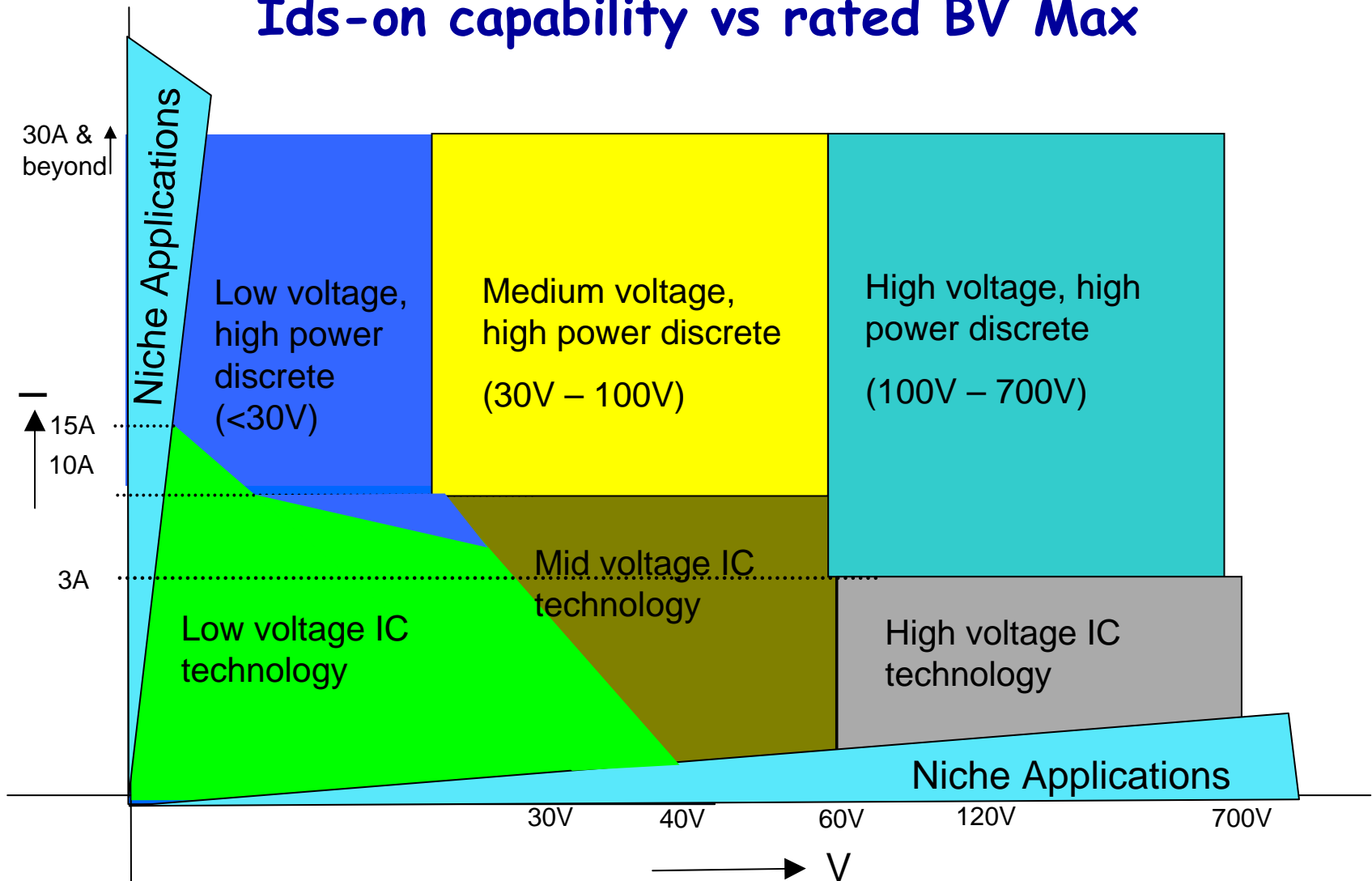
More on Packages

- Trend to move to Copper wire bonding, - lower resistance and cheaper cost
 - But not compatible with all metal systems for bonding
- Continued reduction in size requires much thermal modeling and understanding of heat transfer
- Thinner package means thinner wafer / die
- Multi – chip modules becoming common
- Package differentiation offers flexibility
- Power density becoming big issue



As chip and package shrink, I and V stay the same for application; hence, electrical power stays the same but power density increases squared and cubed !!!

Ids-on capability vs rated BV Max



- For high current above 15-20A most likely monolithic solutions are not cost effective over discrete MCM technology today.

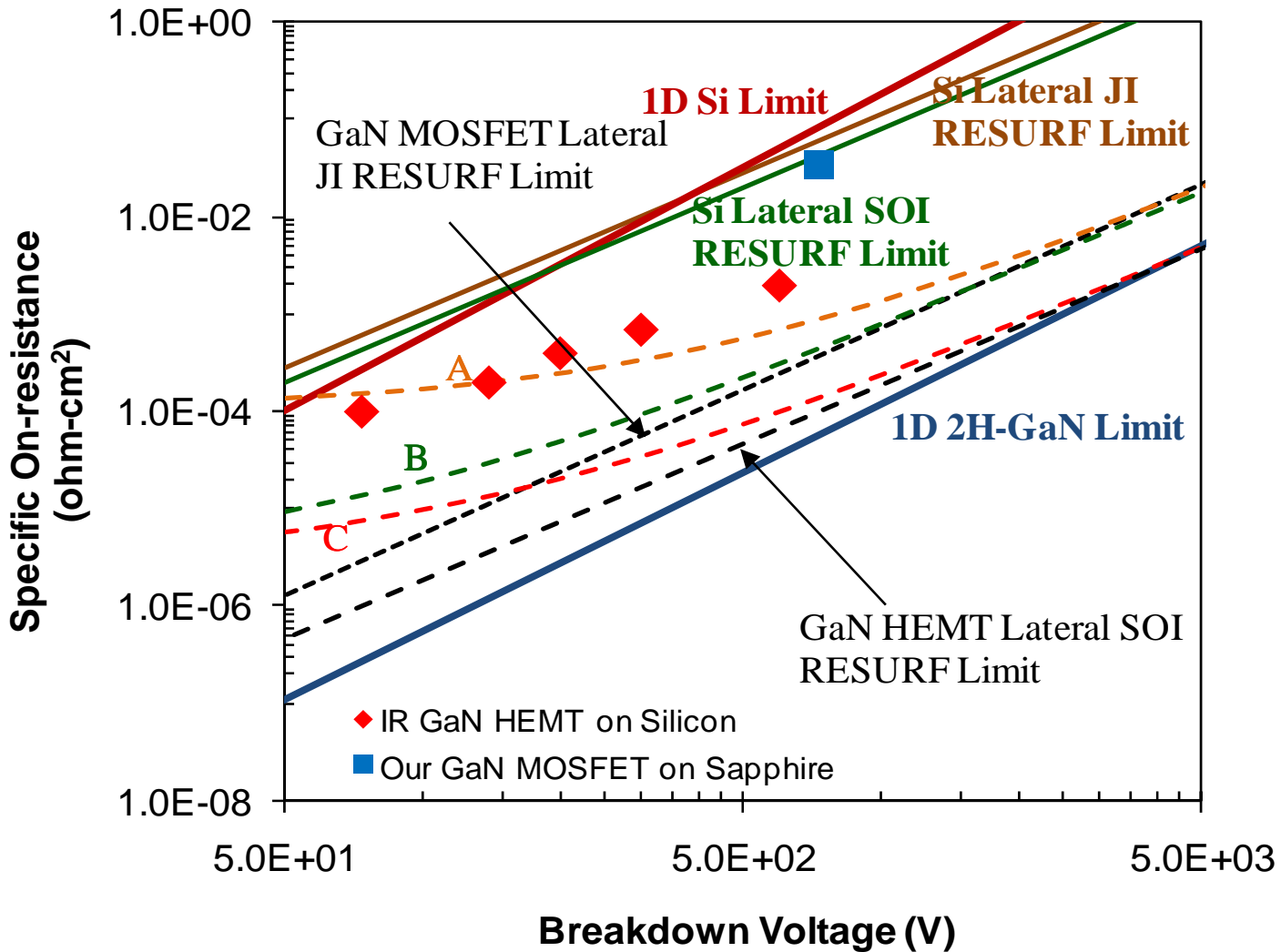
Summary Conclusions

- **Integrated power devices need both great on and off state, and switching efficiency this means low R_{sp} , ultra low quiescent and off state leakage, low Q switching losses**
- **Lower R_{sp} may be reaching a limit that is decided by:**
 - Metal issues and simpler flow options because of cost trade offs
 - Off-State leakage performance
- **Will smaller lithography nodes have any benefit to reducing R_{sp} when facing metal resistance issues?**
 - If not then it is cheaper to stay on the older node
- **Unless**
 - A large digital content drives density need
 - And / or it has to go in a smaller package with the same performance,
 - Or the same package with added functionality

Summary Conclusions

- **Higher switching frequency brings a new set of problems**
 - Can switching losses be managed with device engineering
- **Packaging continues to get smaller and thinner**
 - Power density and thermal management is a big issue
 - MCM combined with discretes becoming more of a norm
 - Off-State leakage performance is of great importance
- **How will other materials play a role in power device for higher speed and higher power density?**
 - SiC becoming mature with larger wafers
 - GaN promising but lot of variation in material science

Si/SiC/GaN comparison – FROM RPI (Prof. Chow's group)



Acknowledgement of Co-Workers

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Analog Products, Dallas, Tx, USA
- **David Jauregui, Power Applications Specialist**
Analog Power Products, Bethlehem, PA, USA

**Thank You Very Much
Dongbu HiTech
For Inviting Me
!**