Delta Sigma ADC and DAC for Hi-Fi Audio, and next trend

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Agenda

• Introduction: role of ADC & DAC
• Why Delta Sigma for Hi-Fi Audio?
• Delta Sigma Technology for Audio:
  Key points from AKM history & products
• Next trend: wide band DSM for RF application
  Key points from today’s R&D
• Conclusions
Analog : between Real & IT digital-world

**Real world**
- Human: by ear, by eye
- Measuring: weight, velocity, magnetism, acceleration

**Analog Players**
- Microphone, CCD/CIS
- -> Amp/Filter -> **ADC**
- <- **DAC**
- Speaker, V-monitor
- PLL, Xtal, TCXO: for clocking

**Digital Players**
- **D-Memory:** CD, DVD, HD, Flash, DSP:
- Echo/Noise cancel
- voice recognition
- sound processing
- (Car, Theater, Game)
- image processing
- (Photo, Video, TV)

**IT world**
- Audio, Movie, Video, Photo, Voice,
- Data transfer via RF/Fiber
Analog vs. Digital Signal

Analog Signal = Continuous Time signal in Real World
get small signal, and reject environment noise

Digital Signal = Discrete Time & Quantized signal in Digital World

Signal Band Width (SBW) = \( \frac{fs}{2} \) \hspace{1cm} (fs= sampling rate)

Quantization noise (Qn): \( SQNR = (6N+1.8)dB \) \hspace{1cm} (N=bit num.)

Main Players in Analog area,

• Sensor : pick up signal from real world
• OPamp, Filter, AGC : amplify or filtering
• ADC, DAC : interface between Analog and Digital
• TCXO, PLL, VCXO: generate sampling clocks
ADC & DAC for RF communication

Communication of data (digital) via RF career (fc)
modulate data --> transfer on RF --> de-modulate
Transferred wave = again, continuous time wave

Players in RF transceiver,
Transmit: DAC, IF-Filter, Up-Mixer, Driver/Power-AMP
Receive: LNA, SAW, Down-Mixer, IF-Filter, AGC, ADC
Both: TCXO, PLL-synthesizer (VCO), LO-buffer

Wideband ADC, DAC:
WCDMA = 2MHz, LTE = up to 20MHz
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Why Delta Sigma for Audio: ADC Architectures

• **Delta Sigma**: $>16$bit accuracy, **closed loop**
  - Noise shaping, high Oversampling Ratio (OSR)
    - $\rightarrow$ high accuracy with a few bit, $> 90\text{dB}$ with 1bit
    - $\rightarrow$ Narrow Signal Band Width (SBW), $(1/\text{OSR})*f_{\text{os}}/2$
    - $\rightarrow$ relaxed Anti-Aliasing Filter (AAF) by high OSR
  - Digital Decimation Filter
    - $\rightarrow$ reject Out-of-Band Noise, generate 16bit PCM
  - Linear performance w/o calibration

• **Flash or Pipeline**: High speed, **ENOB = 8 - 12bit**, **open loop**
  - (a) Flash (1 stage) : $2^n$ Comp $\rightarrow$ up to 8bit
  - (b) Pipeline (N stage) : $N*(1\text{ OP} + 2\text{ Comp})$
    - Mismatch & Gain error limits ENOB up to 12bit
    - direction for Higher fs $\rightarrow$ 250M to 500MHz

• **SAR**: Low Cost, Mid-speed, **ENOB = 12 - 16bit(Cal)**, **open loop**
  - need $N$ cycle for $N$ bit conversion $\rightarrow$ $f_s = f_{\text{conv}}/N$
  - 1 Comp + $N$ bit DAC $\rightarrow$ Low cost for 12bit, but expensive for 16bit
Why Delta Sigma for Audio: DAC Architectures

- **Delta Sigma : >16bit accuracy**
  - Digital Delta Sigma Modulator + DAC (a few bits) + Analog post filter
  - Noise shaping, high Oversampling Ratio (OSR)
    - --> high accuracy with a few bit, > 90dB with 1bit
    - --> 1 bit DAC is perfectly linear (no mismatch)
    - or Multi-bit (few bits) with DWA (mismatch is averaged out)
  - Digital Interpolation Filter
    - --> reject Mirrors in digital domain, relax Analog post filter

- **Current steering: High speed, direct current drive**
  - $2^n$ Current Cells (same to FLASH ADC)
    - --> component mismatch limits ENOB < 12bit

- **R-rudder: Low speed (large R will limit speed)**
  - $2^n$ Resistor tap, total R is large (ex, $2^{16} = 65,536$) --> speed limit
  - R-tap mismatch --> Laser trimmed, high cost
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AKM products

More than 20 years, in Delta Sigma ADC/DAC/CODEC & DSP Leader supplier in Hi-Fi Audio market, from Low-End to High-End

• LOW --> Portable, TV, PC, Game, Phone : 90dB, 16bit, fs=48kHz
  Low Power, Low Voltage, Low Cost,
  Multi-function CODEC (Mic, SPK, HP, Equalizer, noise cancel)

• MID --> Home, Car : 100 to 110dB, 20bit, fs= 48 to 192kHz
  High precision with minimum cost,
  2 to 8 channels for Home Theater, Car surround

• High --> Professional : 120 to 123dB, 24 to 32bit, fs= 48 to 192KHz
  Studio Recording Mixer, Musical Instruments, Measurement

• DSP+CODEC : 90 to 100dB, multi-function
  Dolby surround, Hands free talk(noise/echo cancel)
AKM Technology History : for Audio band

• 1bit 4\textsuperscript{th} order ADC (1988,AES) : 96dB, 2chip (SE)
• 1bit 5\textsuperscript{th} order DAC (1990,AES): 98dB, 2chip (SE)
• 1bit 5\textsuperscript{th} order ADC (1992,AES): 110dB, 2chip (FD)
• 1bit 4\textsuperscript{th} order CODEC (1993,CICC): 90dB, 1 chip (FD)
• 2-2 cascade 4\textsuperscript{th} order ADC (1996,CICC): 111dB, 1chip
• 1.5V, 4mW, 4bit 3\textsuperscript{rd} order DAC (1998,ISSCC): 90dB
• 5bit, 3\textsuperscript{rd} order DAC (1999,ISSCC) : 120dB, 1chip (FD)
• 2-1-1, 4bit, 8x-OSR ADC (2000,ISSCC): 90dB, 1.2M\_BW
• 0.6V, 2-2 cascade, ADC (2005,ISSCC): 82dB, switched RC
• 0.8V, 88dB DAC with HP-driver (2006,VLSI)
Principle of delta sigma ADC (Single-loop, 1-bit)

Analog Input

Loop Filter, H(f)

D/A

Fos=64*48KHz (OSR=64)

1bit_PDM

Digital Decimation Filter
- Reject of out-band-noise
- PDM(1bit) ⇒ PCM (16bit)
- Linear FIR
- Only Digital Test

Fs=48kHz
Dout=16bit

Y = (X - Y) H(f) + Q
{1+H(f)} Y = H(f) X + Q
H(f) >> 1 @ low freq.
Y = X + {1/H(f)} Q
{1/H(f)} Q --> small
Y = X + small Qn
For H(f), LPF or Integrator

Y = (X - Y) H(f) + Q

0dB

-100dB

Fs/2 (after decimation)

Fos/2 (ΔΣ output)

0dB

Signal

Quantization noise

Analog noise (kT/C, 4kTR, 1/f)
4th order, 1bit, Single-loop (1988, AES)

4th order, first in WW, AK5326, SNR=96dBA (A-weight), SNDR=93dB
multi Feed-Forward (a1 to a4) --> stable close loop in 4th order
insert Zero (b0) in Signal Band --> Lower Quantization noise in SB
1bit output (1 or 0) --> inherently Linear
64 times oversampling --> no need of Anti-alias filter (until 3MHz)
3um process = ±5V
4th order, 1bit, Single-loop

1 bit output Spectrum, by Simulation

Signal (1.5kHz)

Quantization noise (1bit = -7.8dB)

After Digital Filter (1/64 decimation, 16bit PCM output), measured
SNR= 96dBA, SNDR=93dB

Expand (DC to 48kHz)
Single chip Stereo CODEC, 4th order (1993, CICC)

AK4501 (ADC=90dBA, DAC=90dBA), for portable Audio, 5V single (1.6um)
**Fully differential Analog DSM**

- cancel out digital noise & even harmonics
- $S/N = +3\text{dB up}$ ($S=+6\text{dB}$, $N=+3\text{dB}$)
- FB-DAC: simple selection of +/-path

![Analog Delta-Sigma Modulator Diagram]
Digital 4th-DSM, Analog 1b-DAC + Post Filter

4th-order Digital Delta Sigma

- Input = 64fs_16bit PCM
- Output = 64fs_1bit PDM
- Integrators --> ACCs
- Time Shared by 2 channel
- Noise shaping in digital (determine SQNR)

Analog 1b-DAC, Post filter

- Fully Differential
- 1b-DAC = pass selection
- SC --> Jitter insensitive
- Reduce Out of band Qn
- Dominant Analog performance (kT/C,..)
5th order, 1bit, Single-loop (1992, AES)

5th order, 2 zeros in signal band, Fully Differential, 3um (+/-5V)

AK5389 (18bit): SNR = 106dBA, SNDR = 102dB

AK5390 (20bit): SNR = 110dBA, SNDR = 104dB

shown as S.E., really F.D.

Fig. 4a Switched-Capacitor Modulator
5th order, 1bit, Single-loop

1bit output spectrum, by Simulation

After Digital Filter, 18bit, measured
2-2 Cascaded ADC, 4th order (1996, CICC)

Stability: multi-stage (DS-loop) is cascaded, each can be up to 2nd-order. Stage outputs (Y1, Y2) is summed in NCL, so as to get final output Y

--- Q1 is cancelled, Q2 remains with high order noise shaping
LFB in 1st stage --> no overload w/o Gain scaling --> more SNR, DR
Noise leakage (Q1) is reduced by 2nd-order --> more mismatch tolerance

Noise Cancel in digital

\[ Y_1 = X + NTF1_a \cdot Q1 \]
\[ Y_2 = -Q1 + NTF2_a \cdot Q2 \]
\[ Y = Y_1 + NTF1_d \cdot Y_2 \]

If \( NTF1_a = NTF1_d \), then Q1 is canceled
\[ = X + NTF1 \cdot NTF2 \cdot Q2 \]

4th order noise shaping

Block diagram of 2-2 cascaded ΔΣM with LFB.
2-2 Cascaded ADC: DR=110dB

1.5kHz input @fs=48kHz

Chip (0.7um DPDM)
High End ADC : 123dBA --> 127dBA

AK5394A : SNR,DR =123dBA, S/N+D= 110dB, fs= 54k(x1) - 216kHz (x4) @5V
Cascade + Multi-bit Quantizer + DWA
Next Trial ---> up to 127dBA
120dB multi-bit DAC (1999, ISSCC)

OSR = x64 or x128
3rd order, 31 value, DWA
--> average mismatch
2 tap FIR in SC domain
--> reduce out-of-band Qn

AK439X series:
SNR, DR = 120 - 123 dBA,
S/N + D = 100 - 105 dB,
fs = 54k (x1) - 216 kHz (x4)
5V single
120dB multi-bit DAC: performance & Photo

1kHz, -60dB, @fs=48kHz (SBW=20kHz)

20kHz, -60dB, @fs=192kHz (SBW=80kHz)

SNDR vs. Input level at 1kHz (fs=48kHz)

Chip (0.5um DPDM)
Conclusion(1) : design points for Audio band

Loop topology :
  Single loop  --> need care for Stability,  insensitive to mismatch
  Cascade loop --> basically Stable,  sensitive to mismatch

Quantization bit number :
  1bit  --> Inherently linear,  Total_Qn = -7.8dB,  need high Order or OSR
  multi-bit  --> need DWA,  Total_Qn = -(6n+1.8)dB,  higher SQNR, DR

OSR consideration :
  High OSR  --> need high speed in SC settling, Comp, Digital
  kT/C noise --> reduced to 1/OSR ( ex.,  if OSR=64,  -18dB reduction)

In Band noise :
  Qn is low enough --> Analog noise is dominant (kT/C, 1/f, Thermal)

Out of Band noise :
  ADC : Digital Decimation Filter can reject perfectly
  DAC : not Audible, but should be reduced by Analog Post Filter

\textbf{for ADC}  \Rightarrow every candidate is possible, select depend on purpose
\textbf{for DAC}  \Rightarrow Single loop, multi-bit, low order is better
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ADC is Key for Receiver of Cell phone (GSM, CDMA, LTE), DTV, WLAN, etc.

Signal Band = 2MHz(WCDMA), 6MHz(DTV), 10MHz(WLAN), 20MHz (LTE)

DR = 50 - 75dB, SFDR = 65 - 90dB  \( <---- \) depend on system req.

Wideband DS-ADC with high DR (70 to 80dB):

Blocker can be rejected by Digital Filter \( --- \rightarrow \) omit IF-Filter, relax AGC

Easy system design, Low power/cost, more reliability ...

How to design Wide-band Delta Sigma?

... Basically Narrow-band by oversampling!!
Approaches for wideband Delta Sigma ADC

- **Trial for Lower OSR**: x64 ---> x16 to x8
  
  \[ \text{LTE} = 20 \text{MHz}, \ f_{\text{os}} = 20 \times 2 \times 8 = 320 \text{MHz} (\@\text{OSR}=8) \]  
  --> can use 0.18um

- In band Thermal noise:
  
  \[ \frac{20 \text{MHz}}{20 \text{kHz}} = 1000 = 2^{10} \]  
  --> 30dB larger than Audio band

- Key points from today’s R&D:

  **Continuous Time (CT)**: **including AAF, no fs tracking, jitter sensitive**
  
  1) Gm-C type in single loop: jitter tolerance, SBW=2MHz
  2) Calibration tech in Cascaded: coefficient matching, SBW=18MHz

  **Switched Capacitor (SC)**: **relaxed AAF, fs tracking, Jitter in-sensitive**
  
  3) Noise couple & Time interleave: extra order, Half clock, SBW=4.2MHz
  4) Double Sampling: OSR= like x4 (real=x8), SBW=20MHz(a), 10MHz(b)

**Other Wideband ΔΣADCs from CICC’11(Sep):**
1) Gm-C type CT-DSM, 5th-single loop (Aiba, JSSCC’09)

DR=71dB, SBW=2MHz, OSR=32, fos=128MHz --> for WCDMA
CT loop filter --> work as AAF in front of Quantizer
Gm-C Integrators --> High speed, but VPT dependent
SC-DAC + R --> jitter insensitive (Charge transfer is small @final of Ts)
Replica DAC --> reduce VPT dependency of Gm-C, DAC-R
1) Gm-C type CT-DSM : DR=71dB, SNDR=68dB

-3dB input, SNDR=68dB

2 tone input, -9dB each

DR=71dB

Fig. 13. Measured SNR, SNDR, HD2, and HD3 versus input level.
2) Calibration in Cascaded CT-DSM  (Kamiishi, CICC’09)

- SBW=18MHz, OSR=10, fos=360MHz  -->  2-1-1 cascade with 4bit Quantizer
- Calibration for Time Constant of Gm-C,
  insert Cal_tone before 1st Quantizer, this works as same as Q1,
  change Cap-value until Cal-tone is vanished on Dout (after NCL),
  then, Analog &Digital coefficients are matched so as to cancel out Q1 leakage

Fig. 5. 2-1-1 cascaded CT ΔΣ modulator and time-constant calibration blocks.
3) Noise Couple & Time Interleave in SC-DSM
(K.Lee, ISSCC’08)

Wide SBW = 4.2MHz, OSR=24, fos=200MHz, Quantizer= 15 level
Time Interleaving (use both clock edge) --> f_clock = 100MHz (=fos/2)
☆ SC settling requirement can be relaxed (5ns --> 10ns)
Noise Coupling add extra (1-z^{-1/2}) in NTF --> 2nd + 1st = 3rd order
Noise Couple & Time Interleave: SNDR=79dB

SNDR =79dB, SBW= 4.2MHz, SFDR= 101dB,  3rd order (60dB/dec)
Power=28mW, FOM=0.48pJ/conv·step,  @0.18um
4) Double sampling SC-DSM

Double sampling ---> use OPamp 2 times per clock
Input SC is separate 2 Caps ---> mismatch will be on fos/2, DF can cut off
no alias-down noise in signal path by AAF
FB-DAC is same cap ---> mismatch of 2 Cap will be aliased down from fos/2
4a) Double sampling in Single-loop (J. Chae, CICC’10)

3rd order, single loop, 15 level, @0.18um
SBW=20MHz, OSR=8, fos=320MHz (f_clock=160MHz)
peak SNDR =63dB, DR=64dB, ---> not enough
Power=16mW, FOM=0.35pJ/conv·step

Fig. 7 Power spectral density with a -3.3dBFS sine wave input.
4b) Double sampling in 2-2 cascade (S. Lee, CICC’11)

Double sampling tech. in 2-2 cascaded SC-DSM:

- SBW = 10MHz, OSR = 8, \( f_{os} = 160\text{MHz} \) (\( f_{clock} = 80\text{MHz} \))
- SNDR = 73.8dB, SFDR = 90dB
- Power = 22mW, FOM = 0.27pJ/conv·step, @ 0.18um

![Diagram of the circuit](image)

*Fig. 7. Measured output spectrum with -1.5dBFS sine wave input.*
5) Wideband ΔΣADCs from CICC’11(Sep.)

6 of 7 papers in ΔΣ session were wideband ADC, nice design & topology were presented, but FOM is almost same w/o depend on process node.

- (SC) OPamp stage-sharing in 2-2 cascade, @0.13um
  SBW=5MHz, OSR=13, SNDR=75dB, 18mW, FOM=0.4pJ

- (SC) Comparator based (ZCBC), 1-1-1-1 MASH, @65nm
  SBW=2.5MHz, OSR=8, SNDR=70dB, 4mW, FOM=0.27pJ

- (SC) VCO-based Quantizer for 2nd stage, 1-1 MASH, @0.13um
  SBW=4MHz, OSR=12.5, SNDR=77dB, 14mW, FOM=0.30pJ

- (CT) 4th-order single-loop, 4bit, RC-Integrator, @0.18um
  SBW=32MHz, OSR=25, SNDR=65dB, 47mW, FOM=1.0pJ

- (LC) RF direct Band pass, fc=900MHz, fs=3.6GHz, @0.13um
  SBW=28MHz, OSR=64, SNDR=50dB, 15mW, FOM=1.0pJ
☆ can omit RF mixer, by digital mixing after ADC!
Conclusion(2) : wideband DS-ADC for RF

CT vs. SC (Discrete Time):
started from CT type, using Gm-C Integrator
  --> moving to RC Integrator with developing of wideband OPamp
SC type run after, covering 5-20MHz band, increasing SNDR
  --> more accurate, fs-tracking for multiple use
  --> challenging for Lower OSR, using many type of circuit tech.
    ( already proven in conventional SC-circuit area )

Delta Sigma ADC vs. Pipeline ADC:
  Pipeline: DR= 50 - 60dB, need high order IF-Filter and AGC
  Delta Sigma: DR= 70 - 80dB, FOM=0.3PJ, Blocker rejection in Digital

RF direct Band-pass Delta Sigma ADC:
  omit RF mixer --> attractive for future RF
  LC resonator  --> need tuning, difficult use for fs tracking system

Delta Sigma is now on R&D for >5MHz, but already feasible for <2MHz, change RX architecture for high-performance, low-power & productivity
Final Conclusion
Final Conclusion

- ADC/DAC is key Interface between Real world and IT/Digital world

- Audio-band Delta Sigma was first introduced in 1988, with continuous tech-challenge, leading Digital Audio Market for better human life.

- Wide-band Delta Sigma ADC will make next innovation in RF application, and will contribute for better communication in World Wide.

- Fine process ( < 90n) is attractive for digital & mm-wave, but leaky and low Voltage. For high performance Analog, small-leakage, high-voltage, component mismatch is more important. Designer’s wisdom shall cover the speed drawback of old process.

- AKM designer will continue technology challenge for WW human life.
Thank you for your Attention!

Wonderful Sound World

Asahi KASEI Microdevices Corp.

for Future RF Communication