Current-mode Driving Schemes for AMOLED Display & SIMO PMICs

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  - DFFC Driver
- Feedforward Driving Methods
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- PMIC
Motivation (1/2)

High Contrast

Natural Color

AMOLED
(Active Matrix Organic Light Emitting Diode)

Fast Response

Wide Viewing Angle

Thin

Low Power Consumption
Motivation (2/2)

AMOLED System

1. Massive capacitance in data lines
2. Non-uniform TFT & Luminance

Requirements for Driver
Introduction (1/2)

- Data driving schemes for AMOLED displays

**Digital**
- TRG
- ARG

**Analog**
- Current
- Voltage

**Hybrid**
- PWM

**Driving Scheme**

**Feedback**
- Current
- Voltage
## Data driving schemes for AMOLED displays

<table>
<thead>
<tr>
<th></th>
<th>Analog Voltage</th>
<th>Analog Current</th>
<th>Digital ARG</th>
<th>Digital TRG</th>
<th>Voltage Feedback</th>
<th>Current Feedback</th>
<th>Hybrid PWM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Threshold Voltage Compensation</strong></td>
<td><strong>Good</strong></td>
<td><strong>Good</strong></td>
<td>-</td>
<td>-</td>
<td>Good</td>
<td>Good</td>
<td>-</td>
</tr>
<tr>
<td><strong>Mobility Compensation</strong></td>
<td><strong>Poor</strong></td>
<td><strong>Good</strong></td>
<td>-</td>
<td>-</td>
<td>Good</td>
<td>Good</td>
<td>-</td>
</tr>
<tr>
<td><strong>Driving Speed</strong></td>
<td>Fast</td>
<td><strong>Slow</strong></td>
<td>Fast</td>
<td>Fast</td>
<td>Slow</td>
<td>Medium</td>
<td>Fast</td>
</tr>
<tr>
<td><strong>Driving Accuracy</strong></td>
<td>Medium</td>
<td><strong>Good</strong></td>
<td>Poor</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td><strong>Luminance Uniformity</strong></td>
<td>Bad</td>
<td><strong>Good</strong></td>
<td>Good</td>
<td>Medium</td>
<td>Medium</td>
<td><strong>Good</strong></td>
<td>Medium</td>
</tr>
</tbody>
</table>

*High Speed Analog Current Driving Method*
*High Driving Accuracy & Speed Current Feedback Method*
Part I

Current-mode AMOLED Drivers:
DFFC (Direct-type Fast Feedback Current) Driver
Block Diagram for FFCD

- Conceptual diagrams for Fast Feedback Current Driver (FFCD)

  *Feedback driver: Current sensing & comparison, loop compensator and error amp.*

![Block Diagram for FFCD](image)
Direct-type Fast Feedback Current (DFFC) Driver

- \( V_{B2} < V_{th,OLED} \)
- OLED turns off during feedback loop operation
Delay Reduction from Capacitance

- Move 2\textsuperscript{nd}, 3\textsuperscript{rd} poles to higher freq.
- Wider BW, faster driving speed

**Low output impedance**

**Impedance**

**Data Line Parasitic**

**Feedback Line Parasitic**

\(I_{\text{DATA}}\)

\(V_{B1}\)

\(V_{B2}\)

\(R_{PD}\)

\(\mathbf{\omega}_{P3}\)

\(R_{PF}\)

\(\mathbf{\omega}_{P2}\)

\(C_{PD}\)

\(C_{PF}\)

\(C_{OLED}\)

\(V_{DD}\)

\(M1\)

\(M2\)

\(M3\)

\(M4\)

\(I_{\text{PIXEL}}\)

\(X\)

\(Y\)

\(\omega_{P1}\)
Requirement for Min. GBW

<table>
<thead>
<tr>
<th>Display Resolution</th>
<th>Driving Accuracy</th>
<th>1-Horizontal time ( (T_H) )</th>
<th>Min. Gain-BandWidth ( (\omega_{GB,\text{min}}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>WXGA (1280 X 800)</td>
<td>8b</td>
<td>20( \mu s ) @60Hz</td>
<td>50kHz</td>
</tr>
<tr>
<td>FHD (1920 X 1080)</td>
<td>8b</td>
<td>15( \mu s ) @60Hz</td>
<td>66kHz</td>
</tr>
</tbody>
</table>
Adaptive Freq. Compensation

- Compensation capacitor (\(C_C\)) array
- \(C_C\) from GBW and PM boundary conditions
- Divide 7 ranges according to \(I_{DATA}\)
Loop Gain with Full $I_{\text{DATA}}$ Range

- $\Delta \omega_{P1}$
- $\Delta T_{\text{DC}}$
- $\omega_{\text{GB, min}}$ (50kHz for WXGA)
- Valid Range ($\geq \omega_{\text{GB, min}}$) 165kHz

Gain (dB)

Frequency (Hz)

$I_{\text{DATA}}$ = 10nA
$I_{\text{DATA}}$ = 40nA
$I_{\text{DATA}}$ = 160nA
$I_{\text{DATA}}$ = 640nA
$I_{\text{DATA}}$ = 2550nA

Valid Range

(50kHz for WXGA)
Measurement Result (Data Transition)

- Data current range from 10nA to 2.55μA
- Settling time < 11μs
Part II

Current-mode AMOLED Drivers: TCF (Transient Current Feedforward) Driver
Introduction of the TCC
Realization of the TCC

CL: Column line
ACL: Adjacent column line
Application and Timing Diagram

(Operation timing diagram)

(Panel application)
**Display Panel Emulation:**

(Implementation of the loading and high speed measurement)
Driver Architecture with TCFD and Path Exchanger
Stability

\[
L_{G_{TCFD}} = \frac{1}{A(s) \cdot g_{m,TFT}} \cdot \left( 1 + S \frac{C_{PP}}{g_{m,M1}} \right) \cdot \left( 1 + S \frac{C_{PP}}{g_{m,TFT}} \right) \cdot \left( 1 + S \frac{C_{PP}}{g_{m,M2}} \right)
\]

The loop gain is always below 0 dB
**Verification by Simulation**

\[ LG_{TCFD} \approx \frac{1}{g_{m,TFT}r_{o,IB}} \left( 1 + s \frac{C_{PP}}{g_{m,M1}} \right) \left( 1 + s \frac{C_{PP}}{g_{m,IB}} \right) \left( 1 + s \frac{C_{PP}}{g_{m,M2}} \right) \]

**I_{DATA} effects on the loop gain**

\( I_{DATA} = 50 \text{ nA} \sim 2 \mu \text{A} \)

**C_{PP} effects on the loop gain**

\( C_{PP} = 10 \text{ pF} \sim 50 \text{ pF} \)

**LG < 0dB**!!

\( (I_{DATA} = 100 \text{ nA}) \)
**Driving Speed**

Step responses of the TCF driving

\( V_{PC} = 300 \text{ mV}, \text{Load} = 6 \text{ kohm}, 40 \text{ pF}, \text{SCAN} = 5 \mu\text{s} \)

10 us of driving time and 5 nA error !!!

Error currents at fixed driving time

\( V_{PC} = 300 \text{ mV}, \text{Load} = 6 \text{ kohm}, 40 \text{ pF} \)
Part III

Current-mode AMOLED Drivers: PP-TCF (Push-Pull Transient Current Feedforward) Driver
PP-TCF Data Driver (1/15)

- Conceptual Diagram of Push-Pull TCF Driver
  - Complete push-pull function for output currents
  - PFB gain control for removing undulation phenomena in pixel currents
PP-TCF Data Driver (2/15)

- Detailed Schematic for PP-TCF Driver
PP-TCF Data Driver (4/15)

**Functional Diagram of Prototype Driver IC**

*Various functions for evaluating the performances of PP-TCF driver*

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**Diagram Details:**
- **CLOCK1** feeds into the **PP-TCF Control Logic**
- **Data Selector** takes inputs Data1 and Data2
- **Data Generator** generates 8-bit data
- **Current DAC** provides current output
- **PP-TCF** connects to **Output Switches**
- **AMOLED Panel** with **Load Emulation**
- **5-stage Distributive Network**
- **Gate Controls** for data selection
- **PRC Enable** and **Data Gen. Enable**
- **Out Switch Control** and **Load Selection**
- **VPRC** and **PRC Enable**
- **Output Switches** (OUTA, OUTB)
- **CST**, **CST**, **CST**, **CST**, **CST**
- **DTFT**, **DTFT**, **DTFT**, **DTFT**, **DTFT**
- **AMP1**, **AMP2**
- **ESCAN**, **OLED**, **Y1**, **Y2**, **OSCAN**, **VDD**
- **VDD**, **VDD**, **VDD**

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Positive Feedback Loop (PFB) Gain Control (1)

PFB gain control for removing undulation phenomena in pixel currents
Positive Feedback Loop (PFB) Gain Control (2)

PFB gain control for enhancing pixel current settling (IDATA = 3uA, panel parasitic 2kOhm/ 60pF)

Conceptual Diagram for PFB Gain Control

\[
A_{PFB,DAMP} = A_O \times \frac{A_1}{1 + M \cdot G_{DAMP} \cdot A_1}
= \frac{A_{PFB}}{1 + M \cdot G_{DAMP} \cdot A_1}
\]

Simulation Results

Loop Gain (dB) vs Frequency (Hz)
Positive Feedback Loop (PFB) Gain Control (3)

*Simulated driving waveforms with/without PFB gain control (IDATA = 1 to 5uA, panel parasitic 2kOhm/60pF)*

![Graph showing simulated driving waveforms with and without PFB gain control.](image)
Current Pulling Function for Enhancing Data Current Settlement (1)

Complete push-pull function for output currents
Current Pulling Function for Enhancing Data Current Settlement (2)

Fast current sense block for current pulling operation

Fast Current Sense Circuit

Conv. Current Sense Circuit
Measurement results (1)

Pixel current settling times improved by current pulling function (IDATA transitions from 4.98μA to 60nA, VPRC= 0.4 to 1.2V, 0.2V step, panel parasitic 4kOhm/90pF)

No Substantial Delays in Data Settlement

Delays in Data Settlement
Measurement results (3)

Waveforms for various data current levels: High to low transitions and low to high transitions of data currents (data current = 20nA to 4.98uA, $V_{PRC} = 0.7V$, parasitic load = 4kOhm/90pF)
## Performance summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.35 μm CMOS (1P 4M)</td>
</tr>
<tr>
<td>Operation voltage</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Data current range</td>
<td>20 nA to 4.98 μA</td>
</tr>
<tr>
<td>Gray scale</td>
<td>8 bit (16.8 million colors)</td>
</tr>
<tr>
<td>Maximum driving load</td>
<td>4 kΩ / 90 pF (Full-HD)</td>
</tr>
<tr>
<td>(Panel parasitics)</td>
<td></td>
</tr>
<tr>
<td>Settling time</td>
<td>≤ 6 μs</td>
</tr>
<tr>
<td>Static current</td>
<td>4.5 μA / Channel</td>
</tr>
<tr>
<td>Occupation area</td>
<td>60 × 308 μm² / 2 Channels</td>
</tr>
</tbody>
</table>

- Appropriate for FHD AMOLED displays
  - Low power consumption
  - Stable operation at high data currents
Part IV

Real-time Image Sticking Compensation using Current Driving
OLED Degradation

- Differential aging dependent on sub-pixel.
- Prolonged display of static image (burn-in)
- RGB have different degradation curves.
<기존 전압 구동용 IS 보상회로>

✓ TFT variation 문제를 해결하더라도, OLED 소자 자체의 시변 열화 특성으로 인해 잔상(Image Sticking)효과를 유발.
✓ OLED의 양단 전압이 열화에 따라 증가하는 현상을 이용한 Electrical Feedback 방식이 연구되고 있음.
✓ 기존 연구 방식들은 모두 전압 구동용 보상회로
OLED Degradation Sensing

\[
V_{\text{diff}} = 2V_{\text{OLED, anode}_1} - V_{\text{OLED, anode}_2}
\]

\(
\alpha: 0 \sim 127
\)

No degradation

Maximum degradation

\[
V_{\text{diff}}\text{ (max)} = \frac{127}{254}\times V_{\text{ref}}
\]

\[
V_{\text{diff}}\text{ (min)} = \frac{0}{254}\times V_{\text{ref}} = 0
\]

\[
V_{\text{diff}} = \alpha V_{\text{ref}}
\]
### IS 보상 방식 비교

<table>
<thead>
<tr>
<th></th>
<th>Compensation Method using Voltage Driving</th>
<th>Real-time Compensation using Current Driving</th>
</tr>
</thead>
<tbody>
<tr>
<td>보상전류</td>
<td>별도의 큰 전류</td>
<td>작은 데이터 전류</td>
</tr>
<tr>
<td>열화 가속</td>
<td>Fast</td>
<td>Slow</td>
</tr>
<tr>
<td>메모리 크기</td>
<td>Large (Vth, μ, OLED)</td>
<td>기존의 1/3 이상 감소 (OLED)</td>
</tr>
<tr>
<td>보상시간</td>
<td>Long time</td>
<td>Real time</td>
</tr>
</tbody>
</table>
- 1:2 DeMUX operation
- Track and Hold type pixel
- TCF driver
- Current DAC with Reference Current Calibrator
Hybrid Data Driver

1. Read data-line voltage by ADC (OLED compensation)
2. Store by line voltage information of each pixel at memory
3. $\phi_1$, VDAC & Amp. pre-charge data-line by pre-stored information.
4. $\phi_2$, CDAC provides data current to pixel. (TFT compensation)
Block Diagram of Hybrid Data Driver

- CDAC sharing scheme
- VDAC = CDAC + I-V Converter
- DATA1 for voltage driving, DATA2 for current driving
Pre-charging voltage is made by using CDAC at each channel.
Digital Processing Algorithm

- DATA1 and DATA2 for hybrid data driving
- \(\alpha\)-LUT for OLED compensation
- Data driving waveforms for various current levels
- High current level (1uA~ 5uA, 1uA step)
- Data driving waveforms for various current levels
- Low current level (5nA~40nA)
Parameter Variation with Degradation Rate

- Changes of $I_{DATA2}$ and $\Delta V_{OLED}$ by compensation algorithm
- $I_{DATA2} @ \alpha=0\% = 100nA$
Summary

- **Feedback (DFFC) driver**
  - Range of data currents from 10nA to 2.55uA
  - WXGA-sized panel load of 1.5kOhm/100pF.

- **Feedforward (TCF, ITCF, PP-TCF) drivers**
  - Full range of data currents from sub-10nA to 5μA
  - Various panel load condition from XGA to FHD-sized panel

- **Real-time image sticking compensation methods**
  - Compensate the luminance degradation of OLEDs
  - Compensate the variation of the driving TFT by current driving
PMIC

Single-Inductor Multiple-Output (SIMO) DC-DC Converters

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Motivation (1)

**Why Multiple On-Chip supply ?**

- Different blocks require different supplies
- AMOLED display requires multiple supplies
- Voltage Scheduling scheme for effective power saving in digital circuit
- Performance improvement in analog & mixed signal systems
Background (1) – Boost converter and LDOs

- Advantages
  - Simple
  - Low ripple
  - Short time-to-market

- Disadvantages
  - Voltage drop → Low efficiency
Why SIMO converter?

- Single inductor: fewer magnetic components, fewer IC pins, lower cost, higher integration
- Fewer on-chip power devices

→ SIMO converter is a cost-effective solution!!
1) Concept of Proposed OPDC

<table>
<thead>
<tr>
<th></th>
<th>PCCM/DCM</th>
<th>OPDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>energy transfer per 1 switching cycle</td>
<td>1 per 1</td>
<td>All per 1</td>
</tr>
<tr>
<td># PI compensator</td>
<td># outputs</td>
<td>1</td>
</tr>
<tr>
<td>Output extension</td>
<td>difficult</td>
<td>easy</td>
</tr>
</tbody>
</table>
Existing PWM DC/DC Converters

- Output Voltage Feedback
- Output Cap. and $I_O$ affect the Loop Response
- Compensator Design is NOT EASY

Diagram:

- Switch Network
- Controller
- $G_c(s)$
- Voltage Reference $V_{ref}$
- Inductor $L$
- Capacitor $V_o$
- Resistor $R_L$
- Input $V_g$
- Output $I_o$
SIMO converter with OPDC

- Comparator control method
- Only one PWM controller
- Easy output extension and high power capacity

[Phuc.ISSCC2007, JSSC 2008]
- 4 Positive boosted outputs + 1 dependent negative output
Measurement Results (1) – Normal operation

**DCM**
- Vo1 = 10.2 V
- Vo2 = 7.0 V
- Vo3 = 7.5 V
- Vo4 = 8.0 V

**CCM**
- Vo1 = 10.2 V
- Vo2 = 7.0 V
- Vo3 = 7.5 V
- Vo4 = 8.0 V

**Boundary of DCM/CCM**
## Performance Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.5 µm Bi-CMOS, t-well, 3AL, 1PS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip area</td>
<td>2.9 x 3.0 mm²</td>
</tr>
<tr>
<td>Package</td>
<td>QFN, 24 pins, 5 x 5 mm²</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>2.5 ~ 4.5 V (3.7 V, nominal)</td>
</tr>
<tr>
<td>Inductor/ESR</td>
<td>10 µH / 350 mΩ</td>
</tr>
<tr>
<td>Oscillator frequency</td>
<td>700 KHz (nominal)</td>
</tr>
<tr>
<td>Current ripple</td>
<td>290 mA</td>
</tr>
<tr>
<td>Maximum efficiency</td>
<td>80.8 % @ 450 mW total load power</td>
</tr>
</tbody>
</table>

### Output

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Vo1</th>
<th>Vo2</th>
<th>Vo3</th>
<th>Vo4</th>
<th>VoN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load current (max) (mA)</td>
<td>5</td>
<td>30</td>
<td>30</td>
<td>40</td>
<td>5</td>
</tr>
<tr>
<td>Load regulation (mV/mA)</td>
<td>1.5</td>
<td>0.78</td>
<td>0.5</td>
<td>0.4</td>
<td>x</td>
</tr>
<tr>
<td>Line regulation (mV/V)</td>
<td>58</td>
<td>73</td>
<td>85</td>
<td>90</td>
<td>80</td>
</tr>
<tr>
<td>Output ripple (max) (mV)</td>
<td>160</td>
<td>140</td>
<td>140</td>
<td>120</td>
<td>200</td>
</tr>
<tr>
<td>Filtering capacitor/ESR (µF/mΩ)</td>
<td>4.7/300</td>
<td>4.7/300</td>
<td>4.7/300</td>
<td>4.7/300</td>
<td>1/150</td>
</tr>
</tbody>
</table>
2) Proposed SIBO converter

- Boost converter
- Adjustable charge-pump

- 2 inductors, 4 switches
- Two PI-control
- Bulky & Expensive

- 1 inductor, 3 switches
- Cost effective
- \( V_{OP} \): Comparator control
- \( V_{ON} \): PI-control
Implementation of SIBO converter

[Chae. ISSCC2007, JSSC 2009]

- Modified Comparator Control (MCC) based on OPDC
$V_{OP}$ control (Modified Comparator Control)

Path 1: Fast error correction

Path 2: Steady-state error correction

$S_{MN}$

CINP

CINN

$X_1$

$S_{VP}$

$M_{p1}$

$V_{OP}$

$C_{OP}$

Channel Control

$X_1$

$t$

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**Measurement Results (1) – Normal operation**

**DCM operation**

\[ I_{OP} = I_{ON} = 20 \text{mA} \at \ V_g = 3.7 \text{V} \]

Freewheel switching

**CCM operation**

\[ I_{OP} = I_{ON} = 35 \text{mA} \at \ V_g = 3.7 \text{V} \]

No Freewheel switching
## Performance Summary

<table>
<thead>
<tr>
<th>Process</th>
<th>0.5μm Power BiCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip area</td>
<td>4.1mm²</td>
</tr>
<tr>
<td>Battery voltage range</td>
<td>2.7~4.5V (3.7V, nominal)</td>
</tr>
<tr>
<td>Inductor / ESR</td>
<td>4.7μH / 320mΩ</td>
</tr>
<tr>
<td>Oscillator frequency</td>
<td>1MHz (nominal)</td>
</tr>
<tr>
<td>Maximum efficiency</td>
<td>82.3%</td>
</tr>
<tr>
<td>Current ripple ΔI</td>
<td>240mA</td>
</tr>
<tr>
<td>Output voltages</td>
<td>V_{OP} (4.58V)</td>
</tr>
<tr>
<td></td>
<td>V_{ON} (-6.24V)</td>
</tr>
<tr>
<td>Output ripples</td>
<td>15mV</td>
</tr>
<tr>
<td></td>
<td>5mV</td>
</tr>
<tr>
<td>Load regulation</td>
<td>0.25mV/mA</td>
</tr>
<tr>
<td></td>
<td>1mV/mA</td>
</tr>
<tr>
<td>Line regulation</td>
<td>6mV/V</td>
</tr>
<tr>
<td></td>
<td>18mV/V</td>
</tr>
<tr>
<td>Filtering capacitors / ESR</td>
<td>4.7μF / 20mΩ</td>
</tr>
<tr>
<td></td>
<td>4.7μF / 20mΩ</td>
</tr>
</tbody>
</table>
3) Freewheeling Current Regulation

- Freewheeling Current Feedback
- Output is Comparator-controlled

- Output Cap. and Load Current do NOT affect the Loop
- Compensator Design is EASY
## Pros and Cons

<table>
<thead>
<tr>
<th>Control Scheme</th>
<th>Loop Dynamics</th>
<th>Main Features</th>
</tr>
</thead>
</table>
| **Direct Duty Control** w/ Output Voltage Feedback | $L, C_o$ | - Complex Compensation  
- Slow Response |
| **Current Mode Control** w/ Output Voltage Feedback | $L, C_o$ | - Difficulty in Compensation for a Wide Load Range |
| **Current Mode Control** w/ Freewheeling Current Feedback | $L, C_o$ | + Load Independent  
+ Simple Wide-Bandwidth Control  
- Power Switch for Freewheeling  
- Small Decrease in Efficiency |
Control of Multiple Output Converter

- No. of outputs can be increased easily

\[ G_{cf}(s) \]

\[ V_{o1}, V_{o2} \]

\[ V_{ref1}, V_{ref2} \]

\[ I_{f}, I_{fs}, I_{offset} \]

\[ M_f, M_n, L \]

\[ V_g, V_n, V_{nb} \]
Measured Waveforms

**Load Transient**

- $I_o$: 100mA to 0A
- $V_{op}$: $V_{pp} < 100mV$
- $V_{op,ac}$: $T_s < 20\mu s$
- $I_L$: Transient response

**Specifications**

- **Ch1**: Freq 2.501kHz, Ampl 100mA
- **Ch3**: Mean 4.01V
- **Ch4**: 200mA

**Scope Settings**

- Channel 1: 100mA, 2.00V
- Channel 2: 500mV, 200mA
- Channel 3: 50.00%
Measured Waveforms

$V_{op} = V_{on} = 23\text{mA}$
## Measured Performance

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.5µm Power BiCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>3.2mm²</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>3.7V nominal (2.7 ~ 4.5V)</td>
</tr>
<tr>
<td>Inductor / ESR</td>
<td>10µH / 350mΩ</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>1MHz</td>
</tr>
<tr>
<td>Filtering Capacitor</td>
<td>10µF Tantal // 470nF Ceramic</td>
</tr>
<tr>
<td>Maximum Efficiency</td>
<td>81% *</td>
</tr>
<tr>
<td>Load Transient (No Load to 100mA)</td>
<td>$V_{o,pp} &lt; 100mV, T_s &lt; 20µs **</td>
</tr>
</tbody>
</table>

* 82.3% achieved in [Chae, ISSCC07].
** These values do not represent the best achievable results.
4) Vestigial Current Regulation

(Seol, ISSCC09)

- Auxiliary Output VA Feedback
- Output Cap. and $I_O$ affect the Loop Response (LIC)
- Additional components are Needed
Implementation of Multiple Output Converter

- $V_{in}$: 2.8 ~ 4.5 V
- $V_{R\cdot G\cdot B}$: 2 ~ 9 V
- $V_{SP}$: Higher than $V_{R\cdot G\cdot B}$ by 0.5 V (Lower limit 6.3V)

\[ V_{DAC}: \text{Higher than } V_{SP} \text{ by 2V (Lower limit 8.3V)} \]
Output switching control

- Averaging of outputs by simultaneous switching
- Discharging of inductor current by the averaged voltage
- Enforced averaging effect by the charging sharing between outputs
- Chaotic switching is alleviated by the averaging effect

- Slightly different outputs
- Simultaneous Turn on & Sequential Turn off

S1 > S2 > S3 > S4

V₀₁ > V₀₃ > V₀₂ > V₀₄

S₁, S₂, S₃, S₄ on

Average of outputs
Measurements Results

- Normal operating waveforms

VIN = 3.7V, Ref_R,G,B = 6V

VIN = 4.5V, Ref_R,G,B = 2V

<Step up> 4.9V 6.0V

<Step down> 5.7V 2.0V
# Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process</strong></td>
<td>0.5μm 1P3M BiCMOS</td>
</tr>
<tr>
<td><strong>f&lt;sub&gt;SW&lt;/sub&gt;</strong></td>
<td>1MHz</td>
</tr>
<tr>
<td><strong>&lt;i&gt;V&lt;/i&gt;&lt;sub&gt;DAC&lt;/sub&gt;</strong></td>
<td>8 ~ 12V, 20mA</td>
</tr>
<tr>
<td><strong>&lt;i&gt;V&lt;/i&gt;&lt;sub&gt;GP&lt;/sub&gt;</strong></td>
<td>6 ~ 10V, 30mA</td>
</tr>
<tr>
<td><strong>&lt;i&gt;V&lt;/i&gt;&lt;sub&gt;R,G,B&lt;/sub&gt;</strong></td>
<td>2 ~ 9.5V, 25, 25, 45mA</td>
</tr>
<tr>
<td><strong>Accuracy</strong></td>
<td>0.1 % [1.5%]*</td>
</tr>
<tr>
<td><strong>Line regulation</strong></td>
<td>0.05 %/V** [1.04%/V]</td>
</tr>
<tr>
<td><strong>Load regulation</strong></td>
<td>0.01 %/mA*** [0.015%/mA]</td>
</tr>
<tr>
<td><strong>Efficiency</strong></td>
<td>83 % **** [80%]</td>
</tr>
</tbody>
</table>

*[] result of [2] **<i>V</i><sub>IN</sub>= 2.5 to 4.5 V*** 0mA to <i>I</i><sub>load</sub> @<i>V</i><sub>IN</sub>= 3.7 V

**** @<i>V</i><sub>IN</sub>= 3.7 V, Ref=6, <i>I</i><sub>load</sub>=25_R, 25_G, 45_B, 30_GP, 10_DAC
5) Proposed Zero-Order Control

- Loop response is independent of $L$ & $C_0$
- $I_f$ is Zero in steady-state: No decreasing Power Efficiency
- Control Loop is Simple
The Role of $V_{ST}$

- Make $\Phi_P$ go to High even when deficient energy case
- $V_{ST}$ causes small Offset Voltage – corrected by MCC

- $V_{ox}$: 200mV
- Larger than $V_O$’s Ripple
## Pros(+) and Cons(-) - ZOC

<table>
<thead>
<tr>
<th>Control Scheme</th>
<th>Loop Dynamics</th>
<th>Main Features</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>FW Current Control</strong></td>
<td>$L, C_o$</td>
<td>- Extra Energy</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Power Switch for Freewheeling</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Decrease in Efficiency</td>
</tr>
<tr>
<td><strong>Auxiliary Output Voltage Control</strong></td>
<td>$L, C_o$</td>
<td>+ Vestigial Current is returned</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Extra Energy</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Additional Components for VA</td>
</tr>
<tr>
<td><strong>Zero-Order Control</strong></td>
<td>$L, C_o$</td>
<td>+ Balanced Energy</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ No Decrease in Efficiency</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ No Additional Components</td>
</tr>
</tbody>
</table>
Measured Waveforms

Steady State - CCM

- Load = 60mA
- No FW period
Measured Waveforms

Load Transient

$V_{OUT(AC)} \quad V_{pp} < 50\text{mV}$

Load

300mA

60mA

$I_L$

80µs

180µs

80/35
6) PLL based SIMO buck converter

- Switching frequency
  - Constant
  - High

- Switch control
  - Comparator control
  - PMB control

- Bang-bang control
  - Stable
  - Fast and accurate regulation
PMB Control (Vo6)

PMB : *PLL-based Multiple-Output Bang-Bang*

- In-Phase Voltage information of error voltage is reproduced by error amplifier (EA).
- *Hysteresis comparator* is implemented by the inverter and capacitor through the system delay.
Loop Analysis of the switching converter

 PLL control-loop

\[
\begin{align*}
\phi_{\text{ref}}(s) & \quad \sum \quad K_{PD} \quad K_{IP}H_{IP}(s) \\
\phi_{VCO}(s) & \quad 1/s \quad K_{VCO} \\
V_{VCO} & \\
\end{align*}
\]
Waveform at the Steady State

\[ Io_1 = 22\text{mA}, \quad Io_2 = 28\text{mA}, \quad Io_3 = 32\text{mA}, \quad Io_4 = 20\text{mA}, \quad Io_5 = 19\text{mA}, \quad Io_6 = 30\text{mA}. \]

\[ Io_1 = 100\text{mA}, \quad Io_2 = 130\text{mA}, \quad Io_3 = 100\text{mA}, \quad Io_4 = 130\text{mA}, \quad Io_5 = 127\text{mA}, \quad Io_6 = 111\text{mA}. \]
7) Proposed SIBBIF Converter (Architecture)

Hybrid Energy Transfer Media

- \( V_g \): Li-ion battery (2.7V ~ 4.5V), USB (5V)
- \( V_{OP} \): 4.6V by boost or buck operation
- \( V_{ON} \): -5.4V by inverting flyback operation
Calculated peak current comparison

\[ i_{pk\_SIBO} = \sqrt{-2T_S (V_{ON} - V_{OP}) < i_{load} >} \]

\[ i_{pk\_SIBBIF} = \sqrt{-2T_S (2V_g + V_{ON} - V_{OP}) < i_{load} >} \]
Simulated efficiency comparison

Efficiency (%) vs. Load Current (mA)

- Proposed SIBBIF Converter
- Previous SIBO Converter

Enhanced efficiency
Multi Level Gate Driver

MLGD is to reduce switching loss

- To reduce the conduction loss, $V_{GS}$ is applied as large as possible
- It inevitably increases switching loss

Conventional Gate Driving

\[(1) P_{SW} = C_g \times V_g^2 \times F_S\]

Multi Level Gate Driving

\[(2) P_{SW} = C_g \times \left(\frac{1}{2} V_g\right)^2 \times 2F_S\]
Multi Level Driving Voltages

Gate voltage of $S_{PM}$:
- $V_{OP}(4.6V)$
- $V_g(3.7V)$
- GND
- $V_{ON}(-5.4V)$

Gate voltage of $S_{PA}$:
- $V_{OP}(4.6V)$
- $V_g(3.7V)$
- GND
- $V_{ON}(-5.4V)$

Gate voltage of $S_{NM}$:
- $V_{OP}(4.6V)$
- $V_g(3.7V)$
- GND
- $V_{ON}(-5.4V)$

Time

$V_{ON}(-5.4V)$
$V_{OP}(4.6V)$
$V_g(3.7V)$
GND
Multi Level Gate Driver for $S_{PM}$

Switch Size: $S_{PM} > S_{PA} > S_{NM}$

$V_g = 3.7V$

$V_{ON} = -5.4V$

$V_{ON}$

$C_F$

$C_{OP}$

$C_{ON}$

$D1$

$V_{ON}$

$S_{PM}$

$S_{PA}$

$S_{NM}$
Multi Level Gate Driver for $S_{NM}$

Body bias of the $M_{P1}$ and $M_{P2}$ is selected as the largest voltage between $V_g$ and $V_{OP}$.
Measurement Results

V_g = 3.7V no load (Pulse skip)

V_g = 3.3V load = 30mA (DCM)

V_g = 4.2V load = 100mA (CCM)

V_g = 5.0V load = 290mA (CCM)
## Performance Summary

<table>
<thead>
<tr>
<th>Process</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supple voltage</td>
<td>2.7V to 4.5V &amp; 5V (USB)</td>
</tr>
<tr>
<td>Frequency</td>
<td>1.25 MHz</td>
</tr>
<tr>
<td>Max efficiency</td>
<td>87.1 %@600mW</td>
</tr>
<tr>
<td>Output</td>
<td>$V_{OP}$ $V_{ON}$</td>
</tr>
<tr>
<td>Voltage</td>
<td>4.6V $-5.4V$</td>
</tr>
<tr>
<td>Max Power</td>
<td>3W</td>
</tr>
<tr>
<td>Line regulation</td>
<td>0.3 %/V 0.14 %/V</td>
</tr>
<tr>
<td>Load regulation</td>
<td>0.12V/A 0.2V/A</td>
</tr>
<tr>
<td>Output ripple</td>
<td>50mV@300mA 60mV@300mA</td>
</tr>
</tbody>
</table>
Summary

- New topology about SIMO DC-DC Converter
  - Cost effective solution
  - AM-OLED Display application
  - Focus on high stability
  - Focus on high efficiency

- New control method about SIMO DC-DC Converter
  - Focus load independent stability
Thank You