BD180LV – 0.18 µm BCD Technology with Best-in-Class LDMOS from 7V to 30V

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***Abstract*— 0.18µm BCD technology with the best-in-class nLDMOS is presented. The drift of nLDMOS is optimized to ensure lowest Rsp by using multi-implants and appropriate thermal recipe. The optimized 24V nLDMOS has BV_{DSS}=36V and Rsp=14.5 mΩ·mm^2. Electrical SOA and long-term hot electron (HE) SOA are also evaluated. The maximum operating voltage less than 10% degradation of on-resistance is 24.4V.**

I. INTRODUCTION

Power management area is one of the highly growing markets in the semiconductor industry. Recently BCD (Bipolar-CMOS-DMOS) technology has been widely used for various applications having large logic contents with power management functions [1-2]. As more logic contents is merged with power function in one chip, designers want BCD process to have more and more dense logic such as 0.18um or 0.13 µm BCD [3]. One can shrink the size of logic transistor by adapting more dense technologies but the size of the high-voltage devices can not be easily reduced due to the fact that the given breakdown voltage needs a resistive area that can sustains high voltage in the off-state. The higher voltage they use, the bigger the resistive region is needed. We have a trade-off between the breakdown voltage (BV) and the on-resistance. In addition, efforts to reduce the on-resistance would be a conflicting reverse direction for the reliability [5]. Therefore, we have to not only design the LDMOS to have very good Rsp (specific on-resistance) at a given BV but also satisfy reliability requirements. In this paper, we present the new technology called 'BD180LV' which is 0.18 µm BCD technology with optimized LDMOS from 7V to 30V. The optimized LDMOS transistors have best-in-class Rsp and good reliability characteristics as well.

II. PROCESS SUMMARY

Starting material is a p-epi on P^+ substrate. NBL (N^+ Buried Layer) is formed on it using Sb (antimony) implants. NBL is used for vertical NPN transistor (collector), high-side LDMOS, and isolated devices. Then, the p-type epitaxial layer, with an appropriate doping concentration and a thickness, is grown on NBL. In the process, 5V NWELL and 5V PWELL are used for body and drain of the DE (Drain-Extended) CMOS. For the nLDMOS optimization, we used dedicated NDT mask to form drift regions. Fig. 1 shows the cross-sectional view of the 24V nLDMOS. We optimized the drift region by using multi-implants of n-type and p-type dopants at the same masking step.

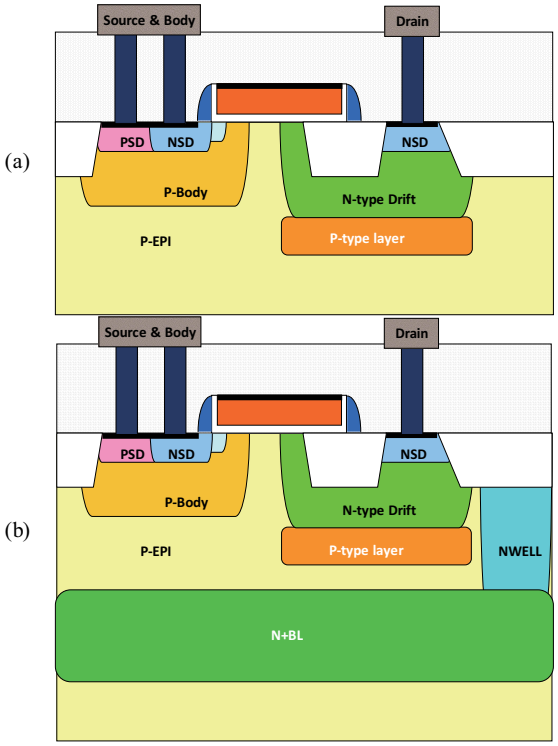

Fig. 1. Cross-sectional view of 24V nLDMOS. (a) Low-side nLDMOS (b) High-side nLDMOS

The optimized dose and energy is very important to achieve low on-resistance and high breakdown voltage. In this technology, the bottom p-type layer is used to ensure full depletion of the n-type drift region so that we could increase the doping concentration of the N-drift region. The p-body of the LDMOS is formed by using double diffusion technique. The p-body has very short channel length and can achieve high transconductance and the current handling capability.

III. EXPERIMENTAL RESULTS

A. DC Characteristics

As shown in Fig. 1a, low-side nLDMOS doesn't have NBL (N+ Buried Layer) underneath. The source of the low-side nLDMOS should be the same potential as the p-epi (substrate). Otherwise, the high-side nLDMOS, as shown in Fig. 1b, has a NBL which can prevent from the depletion of the drift region when the source tied to the load. Fig. 2 shows the simulated structure and impact ionization rate (Fig. 2a) and the equipotential lines at breakdown (Fig. 2b). The simulated breakdown voltage is 42V and the impact ionization rate is highest at the side of STI near the gate. The doping concentration of the bottom p-type region is very important to ensure full depletion at breakdown. In addition, the overlap spacing between N-drift and STI edge strongly affects the Rsp and the breakdown voltage.

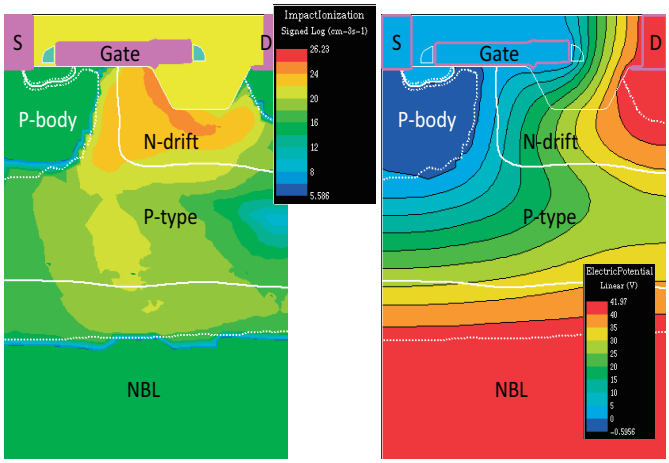

Fig. 2. Simulated LDMOS structure. (a) impact ionization rate and (b) equipotential lines at breakdown (BV=42 V).

Fig. 3 shows the I_{DS}-V_{DS} and breakdown characteristics for the 24V nLDMOS which is measured by HP4156 semiconductor parameter analyzer. The width of 42 µm was used for the measurement and the V_T of 1.0V was obtained. The I_{DS}-V_{DS} curve shows very stable characteristics up to 27.5V and the actual off-state and on-state breakdown voltages are 36V and 33V, respectively. The on-resistance is measured at V_{GS}=5.0V and V_{DS}=0.1V. The specific on-resistance (Rsp) for this 24V nLDMOS is 14.5 mΩ·mm^2, which is the lowest value in the industry.

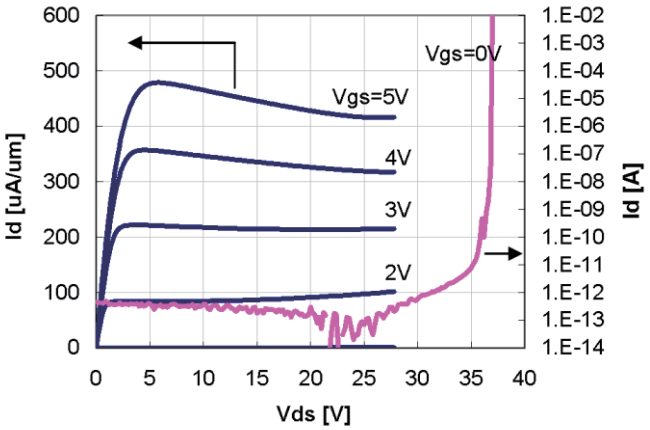

Fig 3. Experimental on-state I_{DS}-V_{DS} characteristics for 24V nLDMOS (Width=42 µm and V_T=1.0V)

In the previous 0.18 µm BCD technology, we had a 24V LDMOS with Rsp of 28.9 mΩ·mm^2. Therefore, the new 0.18 µm technology can shrink 50% of the power transistor area.

Fig. 4 shows the trade-off characteristics between the breakdown voltage and the specific on-resistance. Optimized LDMOS in BD180LV process show the lowest Rsp value compared to the previous publications.

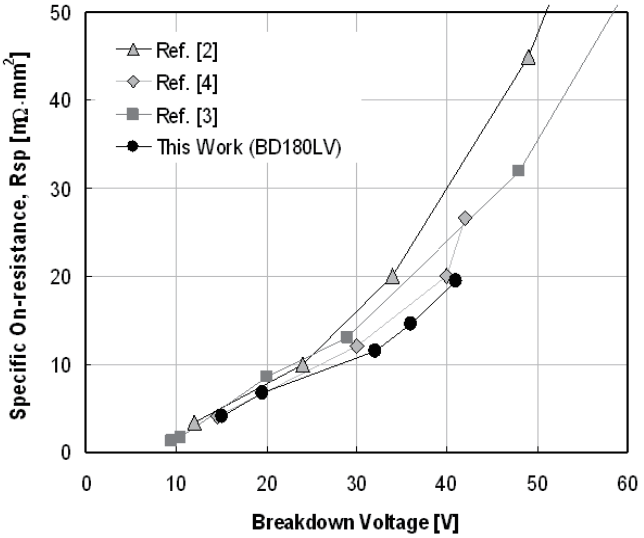

Fig. 4. Trade-off characteristics between the breakdown voltage and the specific on-resistance.

B. Reliability

A reliability of LDMOS becomes more and more important as the Rsp optimization advances [5]. Firstly, we measure the electrical SOA, which is very short term SOA measurement. The LDMOS is measured by using Barth TLP system with pulse width of 100 ns and the rising time of 10 ns. As shown in Fig. 5 the TLP result shows very robust I-V characteristics with V_{DS} up to 30V and gate electric field up

to 4.0 MV/cm. In addition, the I-V curve shows rectangular shape of electrical SOA, which means the drift region is very well optimized.

To further evaluate the reliability for this device, we measured the degradation of the parameters when the high-voltage stress is applied for a long time (up to 100,000 sec). Fig. 6 shows the percentage of parameter drift of the worst-case parameter (Id,lin) at various stress biases such as V_{DS}=27, 28.5, and 32V at maximum gate bias of 5.5V. Fig. 7 shows the extrapolated lifetime estimation as a function of inverse of stress voltage. We measured several parameters such as drain saturation current, on-resistance, and V_T. The on-resistance was the worst case parameter in the stress measurement. Fig. 7 shows that the degradation of on-resistance is less than 10% for 10 years when the device is used at maximum operation voltage of 24.4V.

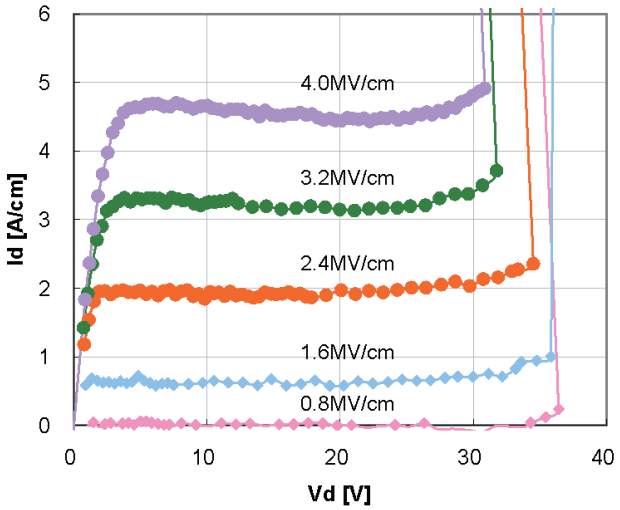

Fig. 5. TLP I-V characteristics for the 24V nLDMOS (Width=42 μm, Threshold voltage V_T=1.0V). The I-V curves are measured by Barth transmission line pulse (TLP) system with pulse width of 100 ns and the rising time of 10 ns.

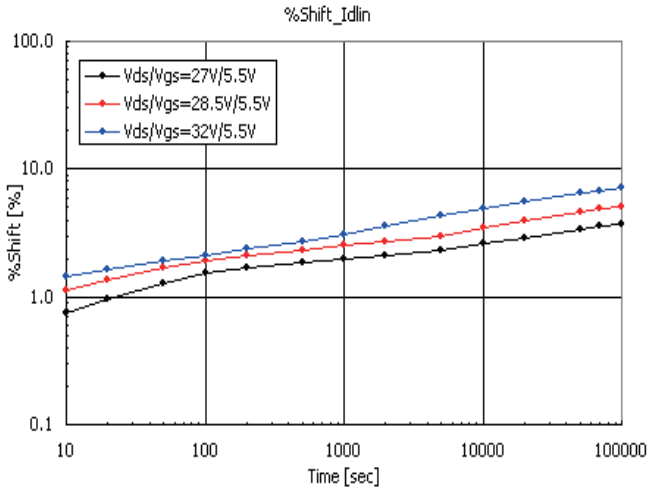

Fig. 6. Worst-case bias stress (V_{GS}=5.5V, V_{DS}=27, 28.5, 32V) degradation for linear-region I_{DS} of the 24V nLDMOS.

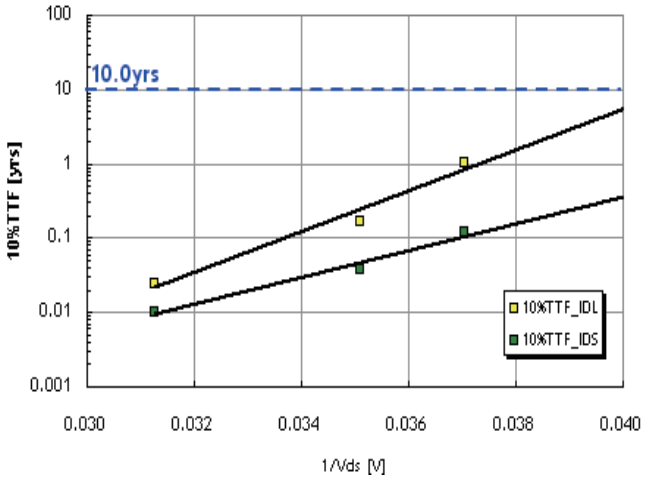

Fig. 7. Lifetime estimation for the 24V nLDMOS.

C. *Other Components*

The BD180LV process has variety of components such as foundry compatible 1.8V and 5V CMOS logic devices, vertical NPN and lateral PNP bipolar transistors, 5.6V Zener diode, 2 KΩ/sq. high sheet rho resistor, and 1.8 fF/μm^2 MIM capacitor. An isolated 1.8V and 5V CMOS are also available and the NBL and HVNWELL are used for isolation guard ring. In addition, we provide drain-extended (DE) CMOS from 7V to 30V for the high voltage circuitry. As a main power device, the process has low-side and high-side nLDMOS devices from 7V to 30V. The key electrical specifications are summarized in Table 1.

TABLE 1. KEY ELECTRICAL SPECIFICATIONS FOR CMOS, BIPOLAR, DIODE, PASSIVES, AND EEPROM.

CMOS	V_T [V]	I_{DSAT} [μA/μm]	I_{off} [Log(A/μm)]
1.8V NMOS	0.42	590	10.7
1.8V PMOS	-0.48	-260	10.7
5V NMOS	0.7	560	13
5V PMOS	-0.7	-280	13
Bipolar	**Hfe**	**BV_{CEO} [V]**	**BV_{CBO} [V]**
8V VNPN	63	12	34
20V VNPN	58	31	40
10V LPNP	184	20	26
20V LPNP	142	28	34
Diode	**V_F [V]**	**V_R [V]**	
Zener	0.7	5.6	
Resistor	**Res. [Ω/sq.]**		
Poly High Rs	2000		
Poly Med. Rs	250		
Capacitor	**Density[fF/μm^2]**	**BV [V]**	
MIM	1.8	21	
EEPROM	**Program Vt[V]**	**Erase Vt[V]**	
Single poly	4.1	-0.5	

(a)

(b)

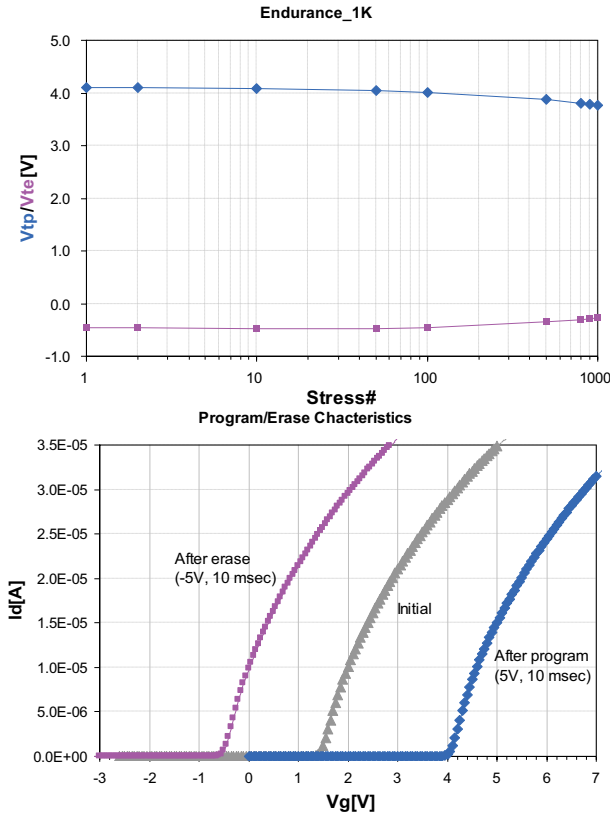

Fig. 8. Endurance test results (a) and cell V_T characteristics (b) for the single-poly EEPROM.

A single-poly EEPROM is often used for trimming purpose with few program/erase cycles in power management ICs. The BD180LV provides a single-poly EEPROM without any change and additional mask from the baseline process. Fig. 8 shows the endurance test results and the program/erase cell V_T characteristics for the single-poly EEPROM. A floating poly forms the gate of NMOS and the top plate of the coupling capacitor. The PWELL of NMOS is isolated by HVNWELL and NBL from the PWELL of coupling capacitor. Because the PWELLs are isolated, we can use +/- 5.5V for programming and erase of the cell. Therefore, they can build a periphery to drive the EEPROM by using only 5V CMOS logic circuit. Thus, the IP size can be reduced due to the fact that there is no need of high-voltage transistor for driving the bit cell.

IV. CONCLUSION

The new BCD technology with very low Rsp LDMOS was introduced. The DC and reliability characteristics for the 24V LDMOS were discussed. The 24V LDMOS showed BV_{DSS}=36V and Rsp=14.5 $m\Omega \cdot mm^2$, which are the best-in-class Rsp performance in the industry. For reliability, we measured electrical SOA and hot electron (HE) SOA. The extrapolated lifetime showed that the maximum operation voltage less than 10% degradation of worst case parameter is 24.4V.

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